EXHIBIT 1

UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., an Irish corporation, Plaintiff, v. LG DISPLAY CO., LTD., a Korean corporation; LG ELECTRONICS, INC., a Korean corporation; and SONY CORPORATION, a Japanese corporation, Defendants.	**CASE NO. 6:19-CV-00236-ADA** **JURY TRIAL DEMANDED**

DECLARATION OF DOUGLAS R. HOLBERG

TABLE OF CONTENTS

Page

I. INTRODUCTION 1

II. QUALIFICATIONS AND COMPENSATION 2

III. RELEVANT LEGAL STANDARDS 4

IV. LEVEL OF SKILL IN THE ART 5

V. TECHNOLOGY BACKGROUND 5

A. Current and voltage 6
B. Thin Film Transistors 8
C. Circuit Diagrams and Symbols 10
D. Using Voltage to Control Luminance 11

VI. THE ASSERTED PATENTS 12

A. U.S. Patent No. 7,907,137 (the "'137 patent") 12
B. U.S. Patent No. 7,432,891 (the "'891 patent") 12
C. U.S. Patent No. 7,573,068 (the "'068 patent") 14

VII. CLAIM TERMS 15

A. '137 patent 15

1. "A gradation current having a current value" ('137 patent at claims 10, 36) 15

B. '891 patent 22

1. "a third thin film transistor which during driving its gate …" ('891 patent, claims 1, 3) 22
2. "wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode" ('891 patent, claim 3) 26

C. '068 patent 30

1. "formed on said plurality of supply lines along said plurality of supply lines" ('068 patent, claim 1) / "connected to said plurality of supply lines along said plurality of supply lines" ('068 patent at claim 13) 30
2. "patterned together" (Claims 1 and 13) 39
3. "feed interconnections" (Claims 1, 10, 12, 13, 17) 51

I, Douglas R. Holberg, make this declaration in support of Defendants' Claim Construction brief. Any statements I make below based on my own knowledge are true, and I have made based on information and belief are believed to be true. The opinions stated herein are my own.

I. INTRODUCTION

1. I am more than eighteen years of age, and I am a citizen of the United States, currently residing in Texas.

2. I have been retained by counsel for Defendants to provide my opinions as to the meaning of certain terms in the asserted claims of U.S. Patent Nos. 7,907,137 (the "'137 patent"), 7,432,891 (the "'891 patent"), and 7,573,068 (the "'068 patent") (collectively, the "Asserted Patents"), asserted by Solas OLED Ltd. ("Solas") in this action. The parties' terms for construction and proposed constructions are identified in Ex. 27.[1] Based on my analysis and investigation, I have reached certain conclusions and developed certain opinions on the issues that I discuss in this declaration.

3. This declaration is based on information currently available to me. I understand that discovery is still ongoing, and I reserve the right to expand or modify my opinions as my investigation and study continues. I may also supplement my opinions in response to any additional information that becomes available to me, any matters raised by Solas and/or any opinions provided by Solas and/or opinions provided by Solas's expert(s), or in light of any relevant orders from the Court.

4. For the purposes of preparing this declaration, I have reviewed the Asserted Patents, their respective prosecution histories, the parties' exchanges of extrinsic evidence, and the other documents discussed in my opinions below.

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[1] All exhibits are to the supporting Declaration of Blake R. Davis.

5. In forming my opinions, I have considered the documents listed, and my knowledge and experience based upon my work in this area.

II. QUALIFICATIONS AND COMPENSATION

6. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

7. My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas in 1992.

8. I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.

9. I am a named inventor on 40 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer, design manager, Director of Engineering, Chief Technical Officer, V.P. of Engineering, and V.P. of Technology.

10. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years, and I have taught a number of short courses in Germany and Ireland.

11. I am the co-author of the textbook "CMOS Analog Circuit Design" which was published in first edition in 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a "circuit works." It is now in third edition and published in English and

Chinese (first and second edition)—a text widely used throughout the world by new and experienced engineers in industry, and by students in the classroom.

12. Upon graduation from Texas A&M, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated DTMF tone generator which was my first patented invention. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as employee #2, where I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched capacitor technology. While enrolled in the Masters/Ph.D. program at The University of Texas at Austin, I worked on the application of bipolar technology to DRAM sense-amplifier architectures and circuit-simulation algorithms. While at The University of Texas, I also designed and laid out the mask set (*The Holberg Mask Set*) still in use by the fabrication class/lab.

13. Upon graduating with a Ph.D., I went to work for Crystal Semiconductor/Cirrus Logic where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing CCD interface circuits for digital camera applications as well as television encoder chips and CMOS imagers. Upon leaving Cirrus, I started a company developing mixed-signal microcontrollers. I was a founder/CTO/VP Engineering, as well as an individual contributor. While at Cygnal, I designed A/D converters, ΔVbe temperature sensors, I/O cells/pads (both design and layout) as well as many additional miscellaneous circuits. My company was purchased by Silicon Labs where I remained employed as a manager of the microcontroller group, followed by the position of VP of Technology.

14. I have significant experience with the technology described in the Asserted Patents, including resistors, capacitors, diodes, inductors, transistors, transformers, oscillators, operational amplifiers, comparators, general integrated-circuit technology, analog/digital mixed-signal

circuits, device analysis and modeling, floor-planning and layout of integrated circuits, and the tools used to design, and verify integrated circuits (CAD tools). In addition, I have experience with device modeling and characterization which has been applied throughout my career.

15. I am being compensated at an hourly rate of $675. My compensation is not dependent on the substance of my statements in this Declaration or the outcome of this action.

III. RELEVANT LEGAL STANDARDS

16. I am not an attorney. I have been informed by counsel of certain legal standards that apply with respect to claim construction and indefiniteness, and have used those standards, described below in formulating my opinions.

17. I understand that the claims of a patent define the limits of the patent's exclusive rights. In order to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I understand that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent applications, after reading the patent and its prosecution history.

18. Specifically, I understand that claims must be construed in light of and consistent with the intrinsic evidence. Intrinsic evidence, this context, includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office. I understand that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

19. I understand that a claim limitation is indefinite if the claim, when read in light the specification and the prosecution history, fails to inform with reasonable certainty a person of ordinary skill in the art about the scope of the invention.

IV. LEVEL OF SKILL IN THE ART

20. I understand that the factors that may be considered in determining the level of skill of a person of ordinary skill in the art (POSITA) include, but are not limited to, (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) the educational level of active workers in the field.

21. Taking these factors into account, I have concluded that a person of ordinary skill in the art ("POSITA") at the relevant time would have had at least a bachelor's degree in electrical engineering (or equivalent) and at least two years' industry experience, or equivalent experience in circuit design or related fields. Alternatively, a POSITA could substitute directly relevant additional education for experience, e.g., an advanced degree relating to the design of electroluminescent devices, drive circuits, or other circuit design or an advanced degree in electrical engineering (or equivalent), with at least one year of industry experience in a related field, and vice versa.

22. At the time of the alleged inventions, I was a person of at least ordinary skill in the art, and I have applied the perspective of the POSITA in forming and expressing my opinions below.

V. TECHNOLOGY BACKGROUND

23. The three Asserted Patents relate to flat panel organic light-emitting diode ("OLED") displays, where each pixel is formed by organic light emitting diodes. As their name implies, OLEDs are the parts of a pixel that actually give off light. In this context, the pixel also includes a "drive circuit" that controls the amount of light (a luminance gradation or light emitting level), of the OLED. In other words, each OLED has its own drive circuit, and together the OLED

and drive circuit form a pixel. In a given television or computer display, there will be many (often millions) OLEDs arranged in an array along rows and columns of the display screen.

24. For OLED displays, the "luminance" of the light emitted by each individual pixel depends on the strength of the current that flows into the OLEDs. That means that the stronger the current, the greater the amount of light emitted by the OLED will be. The drive circuits of each pixel are used to individually control how much current is supplied to the OLED. Thus, each OLED can be individually controlled to provide differing amounts of light, allowing an image to be displayed.

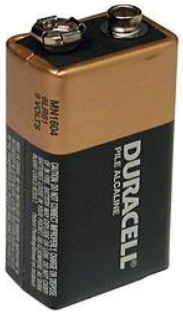
25. The Asserted Patents generally relate to how OLED drive circuits work, and in the case of the '068 patent, how they can be manufactured using conventional integrated circuit manufacturing techniques. Below, I provide a brief background of certain physics and electrical engineering concepts that helps inform the disputes between the parties over the meaning of certain claim terms in the Asserted Patents..

A. Current and voltage

26. To electrical engineers and persons of ordinary skill in the art, current and voltage refer to two distinct but related electrical concepts. "Current" is the rate of charge, or electrons, flowing through a wire or a circuit. Ex. 2 (IEEE 100) (2000) at 257 ("current (1) The flow of electrons within a wire or a circuit"); Ex. 3 (Hargrave's Computer Dictionary) (2001) at 131 ("current The amount of charge (electrons) flowing past a point in a conductor per second."). "Voltage" is the potential energy required to move electrons from one point to another in a circuit. Ex. 2 at (IEEE 100) at 1260 ("volt (metric practice) (unit of electric potential difference and electromotive force) The difference of electric potential between two points of a conductor carrying a constant current"; "voltage (1) (electromotive force)"); Ex. 3 (Hargrave's Computer Dictionary) at 572 ("voltage The amount of energy available to move a certain number of electrons

from one point to another in an electrical circuit."). Voltage is also commonly referred to as "potential," "potential difference," or "electromotive force." Ex. 2 (IEEE 100) at 1260 ("voltage is synonymous with potential difference"); Ex. 4 at 502 (Microsoft Computer Dictionary) ("voltage n. see electromotive force."), *id.* at 172 ("electromotive force … also called potential, voltage").

27. Current and voltage are related to one another according to Ohm's Law. A higher voltage can correspond to a higher current, in a similar way that higher water pressure can result in water flowing faster through the pipe. However, "current" or "voltage" are not the same thing, nor are they interchangeable. For example, voltage can exist without current. To use a familiar example, a 9-volt battery has a specific voltage, or potential energy, but unless and until it is connected to a circuit that allows current to flow, the battery alone supplies no current.

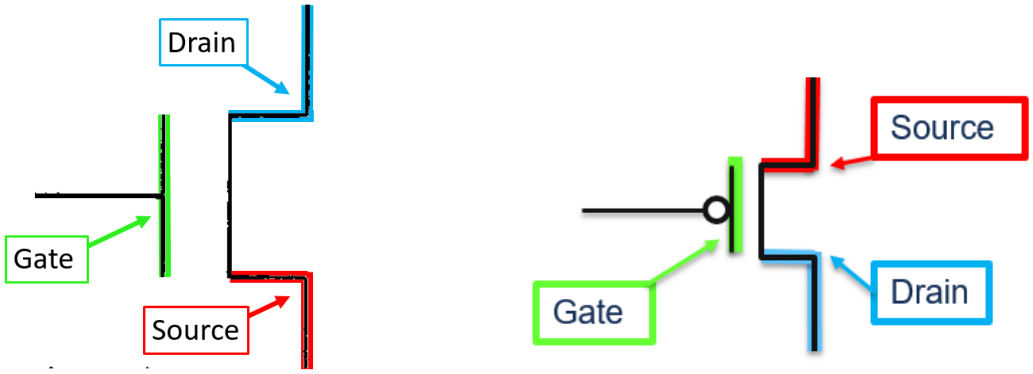


28. To help understand these electrical concepts, current and voltage are often thought of in the more familiar context of water flowing through a pipe. Current is analogous to the rate of water flowing through the pipe. Voltage, on the other hand, is analogous to the water pressure that forces the water through the pipe. Just as voltage and current are different but related concepts, so are water pressure and water flow. A full, closed tank of water, for example, will have a certain water pressure. But no water flows from it unless and until the tank is opened and water is released, like through a valve, pipe, or hose.

29. Voltage and current can be used for different purposes in circuits. For example, circuits can be designed as current-controlled or voltage-controlled depending on the desired architectural goals.

B. Thin Film Transistors

30. A key component of OLED drive circuits are "thin film transistors" (TFTs). Like any transistor, TFTs are circuit components that are made with "semiconductor" materials that can be used to conduct electricity in some situations, but not in others. Silicon, for example, was and is a common and well-known semiconductor material. A TFT, like any transistor, has three electrodes (also referred to as terminals): (1) a gate, (2) a source, and (3) a drain. Below are two ways that TFTs are typically depicted in a circuit diagram.



See, e.g., '891 patent at Fig. 1, '068 patent at Fig. 2.[2]

31. In these transistors, the gate serves to control the flow of current between the source and drain. Specifically, the source and drain electrodes are connected on either side to a

[2] The depicted transistor on the left is what is referred to as an N-channel-TFT, and on the right is a P channel TFT. The Asserted Patents are not limited to any particular type. *See, e.g.*, '891 patent at 2:58-62 (stating that "P-channel-TFTs (T1,T2)" are depicted, but "[n]aturally, also corresponding layouts with N-channel TFTs or CMOS implementations are possible."); '068 patent at 31:42-52; '137 patent at 13:22-30 ("The thin film transistor Tr11 to Tr13 are not particularly limited to any specific type."), 28:34-44).

semiconductor material, like polysilicon. That semiconductor material, depending on a voltage applied to the gate, can act as a conductive "channel" for current (electrons) to flow between the source and drain. The ***amount*** of current that can flow is determined by the difference in voltage between the gate and source (the gate-source, or gate to source, voltage). When the gate to source voltage is below a certain threshold voltage value (the "threshold voltage" specific to that individual TFT), the TFT's channel is nonconductive and no current will flow between the source and drain. When the voltage between the gate and source is above the threshold voltage, the channel becomes conductive and allows current to flow. By further increasing the gate voltage compared to the source voltage, the channel becomes more conductive, allowing greater current to flow between the source and drain.

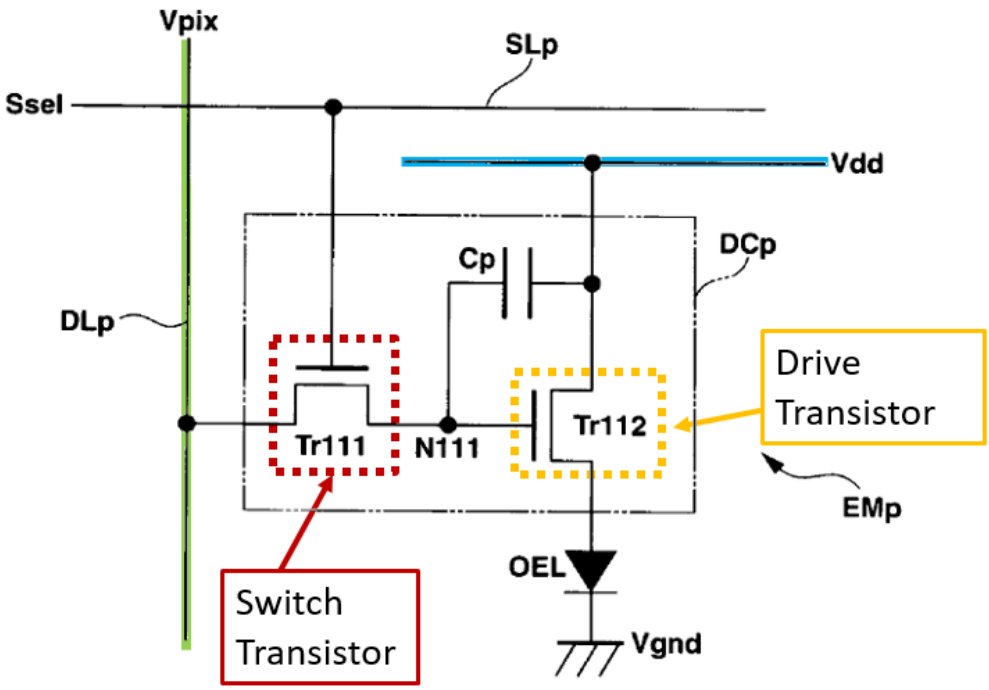
32. A transistor demonstrates one of the fundamental differences between how "current" and "voltage" are used differently in a circuit. Specifically, a transistor uses ***voltage*** at the gate of the transistor to control the ***current*** that flows from the source to the drain. However, while there is a voltage at the gate of the transistor, current cannot flow into or through the gate, as there is no path for electrons to flow. In other words, the gate is like a dead end. A POSITA therefore generally refers to the "source" and "drain" of a TFT as the "current conducting" electrodes, while the gate is a "control electrode." *See also, e.g.*, '891 FH at 149 (explaining that in a TFT, the "current carrying terminals" are the "Drain and Source" and "the gate is not current carrying").

33. Applying these principles, different levels or "gradations" of voltages can be applied to the gate of a TFT so that the TFT allows correspondingly different levels of current to flow through it. Alternatively, a TFT (e.g., an N-channel TFT) can be used as an on/off switch that either blocks current from flowing, or allows all current to flow by applying a low or high

voltage to the gate. In basic terms, when a TFT allows current to flow by applying a voltage to its gate, the transistor is turned on, and when a transistor does not allow current to flow because the gate voltage is too low, the transistor is turned off. Returning the water in pipes analogy, a TFT can be thought of as a valve on the pipe, which can either shut the flow of water on or off, or control the rate at which water flows.

C. Circuit Diagrams and Symbols

34. Engineers and persons of ordinary skill in the art typically describe circuits and their multiple electrical components using schematic circuit diagrams, using conventional, well-established symbols. For example, TFTs are typically shown using the symbols shown above, and conductive lines through which electricity flows are typically shown using solid lines. This is true in the Asserted Patents as well. An example of an admitted "prior art" pixel (EMp), comprising a drive circuit (DCp) and an organic light emitting diode (OEL) is shown in Figure 36 of the '137 patent below.



'137 patent at Figure 36 (annotated); *id.* at 1:59-3:5.

35. As described in the ’137 patent, the “circuit DCp” includes two TFTs, Tr111 and Tr112. Tr111, annotated in red above, has its gate connected to a scanning line SLp, source connected to a data line DLp, and its drain connected to the gate of Tr112 and one side of a capacitor (Cp). ’137 patent at 2:12-16, 2:23-35. Tr112, annotated in yellow, has a gate that is connected to Tr111, and its current conducting electrodes (source and drain) connected between a power supply Vdd and one side of the organic light emitting diode (OEL). *Id.* at 2:16-25. Like the TFTs, the OEL is depicted using a standard “diode” circuit symbol, and has “an anode terminal connected with a drain terminal D” of Tr112, and “a cathode terminal receiving a ground potential Vgnd lower than the power supply voltage Vdd.”. *Id.* at 2:19-23.

36. In the prior art drive circuit shown above, Tr112 is often referred to as a “drive transistor” because, depending on the voltage at its gate, it controls the amount of current that flows from the power supply line Vdd to the OEL. *Id.* at 2:46-52. Tr111 is often referred to as a switching or scan transistor, and switches either on or off to electrically connect, or disconnect, the gate of the drive transistor to the data line DL. *Id.* at 2:42-58.

D. Using Voltage to Control Luminance

37. The prior art circuit above is referred to as a “voltage gradation specification mode (or voltage gradation specification drive)” circuit. This is because the level of current that flows through the driving transistor (the “driving current”) into the OEL, which determines the level of light emitted by the OEL, is controlled using different levels of voltage on the data line corresponding to display data. ’137 patent at 3:6-14. Specifically, the voltage level that controls the light emitting level of the OEL is a “voltage value corresponding to display data,” labeled Vpix in Figure 36 above, and it is provided directly to the gate of the driving transistor Tr112 through the switching transistor Tr111. ’137 patent at 2:34-52. When the switching transistor Tr111 is turned on, it electrically connects the gate of the drive transistor Tr112 to the data line. The circuit

then provides a "gradation ***voltage*** VPix," which has a "value corresponding to display data," from the "data line (signal line) DLp," to the gate of the driving transistor. *Id.* at 2:34-41. The drive transistor then allows a corresponding level of current to flow from the "supply line" Vdd to the OEL, illuminating the OEL. '137 patent at 2:46-49. "[C]onsequently, the organic EL element OEL operates to emit light with a luminance gradation [i.e., a grade of light emission intensity] corresponding to the display data (the gradation ***voltage*** Vpix)." *Id.* at 2:49-52.

VI. THE ASSERTED PATENTS

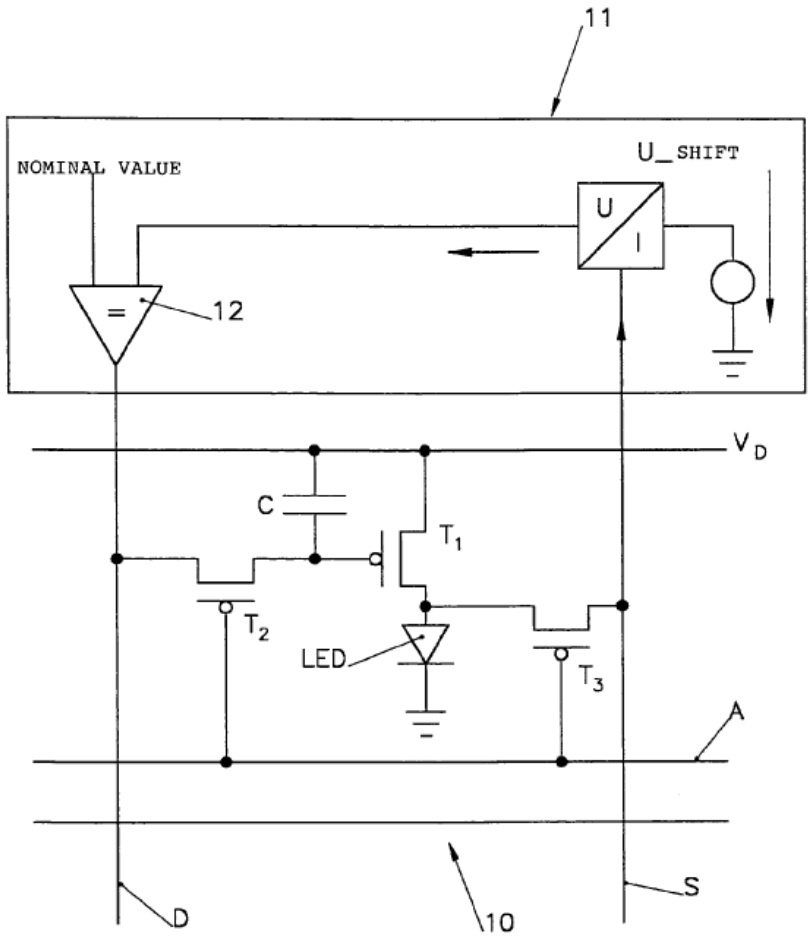
A. U.S. Patent No. 7,907,137 (the "'137 patent")

38. The '137 patent is directed to a ***current-programmed*** OLED display, where ***current***, rather than voltage, is used to control the luminance of the pixels in the display. In the drive circuits of the '137 patent, "a gradation ***current*** having a current value … corresponding to display data" flows "via a data line DL toward a drive circuit DC provided on a display pixel PX." *Id*. at 20:27-53. This is distinct from the "voltage programmed pixels" discussed above, which use a voltage value provided to the data line to control the luminance of the pixel. *See id.* at 2:64-3:5, Fig. 36 (depicting prior art). The claims of the '137 patent also recite other operations that must occur through the same data line where the gradation current is provided, including (1) detecting a threshold voltage, and (2) applying a compensation voltage based on the detected threshold voltage to the drive circuit. The '137 patent explains that the purpose of these detecting and compensating steps is to "precharge" the drive transistor to shorten the amount of time required to program a pixel with its gradation current.

B. U.S. Patent No. 7,432,891 (the "'891 patent")

39. The '891 patent uses a voltage programmed drive circuit, not unlike the one shown in Figure 36 of the '137 patent above. This patent is directed to addressing what it states is a well-known problem, where manufacturing differences between the different drive transistors in an

OLED display can affect the amount of current provided to each OLED, causing different amounts of light to be emitted when the same data voltage is applied to the gate of the transistor. ’891 patent at 1:14-21, 1:22-36 (discussing “driver current fluctuations”). To solve this problem, the ’891 patent claims a driving circuit that adds a third transistor to the basic two-transistor voltage programmed pixel discussed above that is connected to a “current measuring and voltage regulating circuit.” The only figure of the ’891 patent is shown below, which has a first TFT (T1) that “acts as a current driving transistor for the LED element,” a second TFT (T2) that electrically connects or disconnects the gate of T1 to a data conductor D, and a third TFT (T3) connected between the output of T1 and a conductive line labeled S.



’891 patent at Fig. 1, 2:65-12.

40. The claims recite that while the third transistor is turned on, i.e., "during driving" of the third transistor's gate, the "diode driving current" at the output of the current driving transistor, is tapped, supplied to a current measuring circuit, and a correcting "voltage signal" is provided to the data conductor depending on the measured value of the current. '891 patent at 2:11-17. The '891 states that the third transistor is provided "for current feedback," so that, after the third transistor is switched off, the current through the OLED is stabilized. *Id.* at 2:17-18, 3:8 ("for current feedback, the circuit has a third [thin] film transistor T3").

C. U.S. Patent No. 7,573,068 (the "'068 patent")

41. The '068 patent is directed to manufacturing an OLED display that "satisfactorily drive[s] a light-emitting element while suppressing any voltage drop and signal delay." '068 patent at 1:15-20, 2:39-41. Thin film transistors, as the name suggests, are manufactured from thin films of deposited material. An exemplary manufactured TFT with its source, drain, and gate electrodes, is shown below in a cropped and annotated version of Figure 5 of the '068 patent.

42. The '068 patent explains that, conventionally, a supply line that provides current to an OLED through the drive transistor of a drive circuit will be formed in the same layer as either the source and drain electrodes, or in the same layer as the gate electrode. *Id.* at 1:57-2:4. The '068 patent states that when supply lines are patterned with the sources and drains of the TFTs the supply line alone is too thin to provide sufficient current to pixels along it in the horizontal direction. '068 patent at 1:57-2:12; *see also id*. at claims 1, 13 (requiring "plurality of supply lines which are patterned together with the sources and drains"). Specifically, because the supply line is thin, it has a high resistance, causing unwanted voltage drops and interconnection delays when trying to illuminate pixels farther from the source. '068 patent at 2:5-14, 18:26-30 ("The resistance of a thin film such as the gate or the source/drain of a thin-film transistor is so high that the write current (i.e. driving current) cannot be supplied to the organic EL elements 20."). By analogy, a

thin supply line is a narrow pipe for water to flow through, causing problems limiting the current to the pixels across a display. To solve this problem, the '068 patent discloses forming "feed interconnections" in a layer that is different than the one in which the TFT electrodes are formed, allowing the feed interconnections to be thicker and have lower resistance than interconnects formed in the TFT layers. *Id.* at 3:60-4:14, 10:25-32, 18:26-40, 26:62-66.

VII. CLAIM TERMS

A. '137 patent

1. "A gradation current having a current value" ('137 patent at claims 10, 36)

43. The term "a gradation current having a current value" appears in claims 10 and 36 of the '137 patent.

44. The full limitations of claims 10 and 36 that include this term are shown below.

Claim 10

a gradation signal generation circuit which generates a gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of the display data, as a gradation signal corresponding to the luminance gradation of the display data, and supplies the gradation current to the display pixel through a data line connected to the display pixel;

Claim 36

supplying, after the drive element holds the voltage, a gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of display data, as a gradation signal to the display pixel through the data line, adding a voltage component based on the gradation signal to the voltage component based on the compensation voltage, and allowing the drive element to hold the voltage component.

45. In my opinion, the "gradation current having a current value" refers to an actual current with a value corresponding to a luminance level, and not a voltage or value of voltage corresponding to a luminance level.

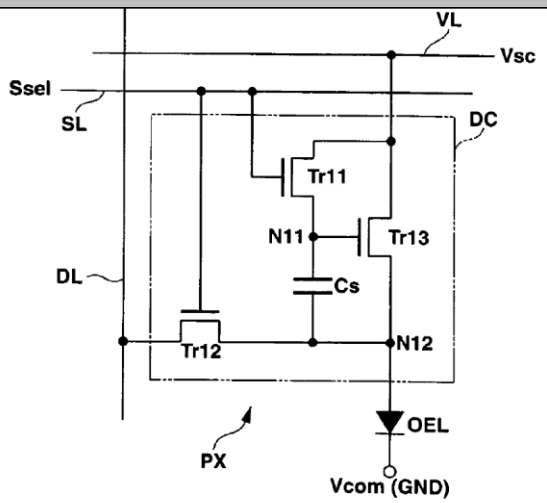
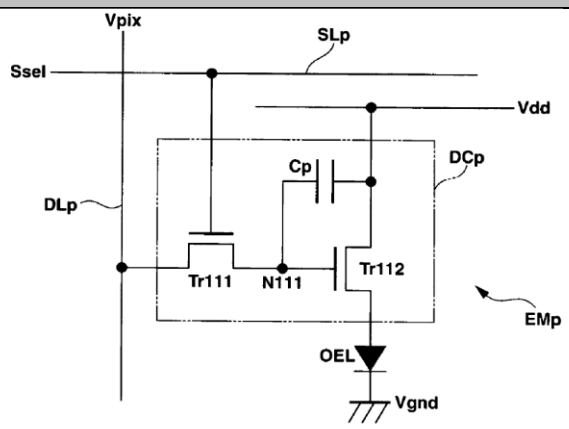
46. A POSITA would have understood in view of the specification that providing a "gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of display data" requires a different drive circuit arrangement than a circuit providing a "gradation voltage" as "a luminance gradation of display data."

47. For example, the '137 patent describes with reference to Figures 35 and 36, which are prior art conventional circuits, a "voltage control" type drive circuit shown below. In this circuit, a "voltage value of the gradation voltage Vpix" corresponding to display data is provided on the data line DLp to the gate of the drive transistor Tr112 through the thin film transistor Tr111. *Id.* at 2:42-52, 3:6-14. The drive transistor then provides a current to the OLED corresponding to that gradation voltage Vpix, and adjusting the gradation voltage Vpix controls the current value of a driving current which flows to the organic EL element OEL. As stated in the '137 patent, "[s]uch a drive control method is referred to as a voltage gradation specification mode (or a voltage gradation specification drive)."

> Such a drive control method is referred to as a voltage gradation specification mode (or a voltage gradation specification drive) since a current value of a driving current which flows to the organic EL element OEL is controlled to perform a light emitting operation with a predetermined luminance gradation by adjusting a voltage value of the gradation voltage Vpix applied to each display pixel EMp (specifically, the gate terminal of the thin film transistor Tr**112** of the drive circuit DCp).

’137 patent at 3:6-14.

48. Unlike a voltage gradation current drive circuit, the ’137 patent’s drive circuits use a “current gradation specification mode (or, a current gradation specification drive) of directly flowing a current component (a gradation current) of a gradation signal.” ’137 patent at 20:29-36. A notable difference in the structure of the current gradation specification drive circuit is that the data line is connected to the ***source*** of the drive transistor, which is a current conducting electrode, through the switching transistor, rather than to the gate of the drive transistor in the voltage gradation specification mode. This allows a gradation current to be provided on the data line to the drive transistor, which is used to control the luminance of the OLED according to display data.

Gradation Current	Gradation Voltage
 FIG.1	 FIG.36 PRIOR ART

’137 patent, Figs. 1, 36.

49. Every embodiment in the specification uses a current gradation specification drive circuit such as the one shown in Figure 1 above. *See, e.g.*, ’137 patent at 21:62-23:14. And the specification repeatedly describes providing a “gradation voltage” as distinct from providing a “gradation current.” *See, e.g.*, ’137 patent at 2:34-41, 2:49-52, 3:6-14, 3:36-41, Figs. 35, 36 (discussing prior art’s use of a “gradation voltage”); *id.* at 14:63-67, 16:3-5, 20:29-36, 22:4-14,

22:19-24, 22:25-32, 24:2-10, 24:30-37, 28:49-60, 38:10-19, 38:53-58, 56:13-17, Figs. 7, 8, 9 (discussing patent's use of a "gradation current").

50. The prosecution history also would have informed a POSITA that a "gradation current having a current value" does not include a voltage programmed circuit. During prosecution, the applicant responded to a rejection based on a prior art disclosure of gradation voltage by amending the claims to limit the gradation signal to a gradation current.

> a gradation signal generation circuit which generates a gradation current having a current value for allowing the optical element to perform a light emitting operation at a luminance corresponding to a luminance gradation of the display data, as a gradation signal corresponding to [[a]] the luminance gradation of the display data, and supplies the gradation ~~signal~~ current to the display pixel through a data line connected to the display pixel;

Ex. 5 ('137 File History) at 2 (August 24, 2010 Claims).

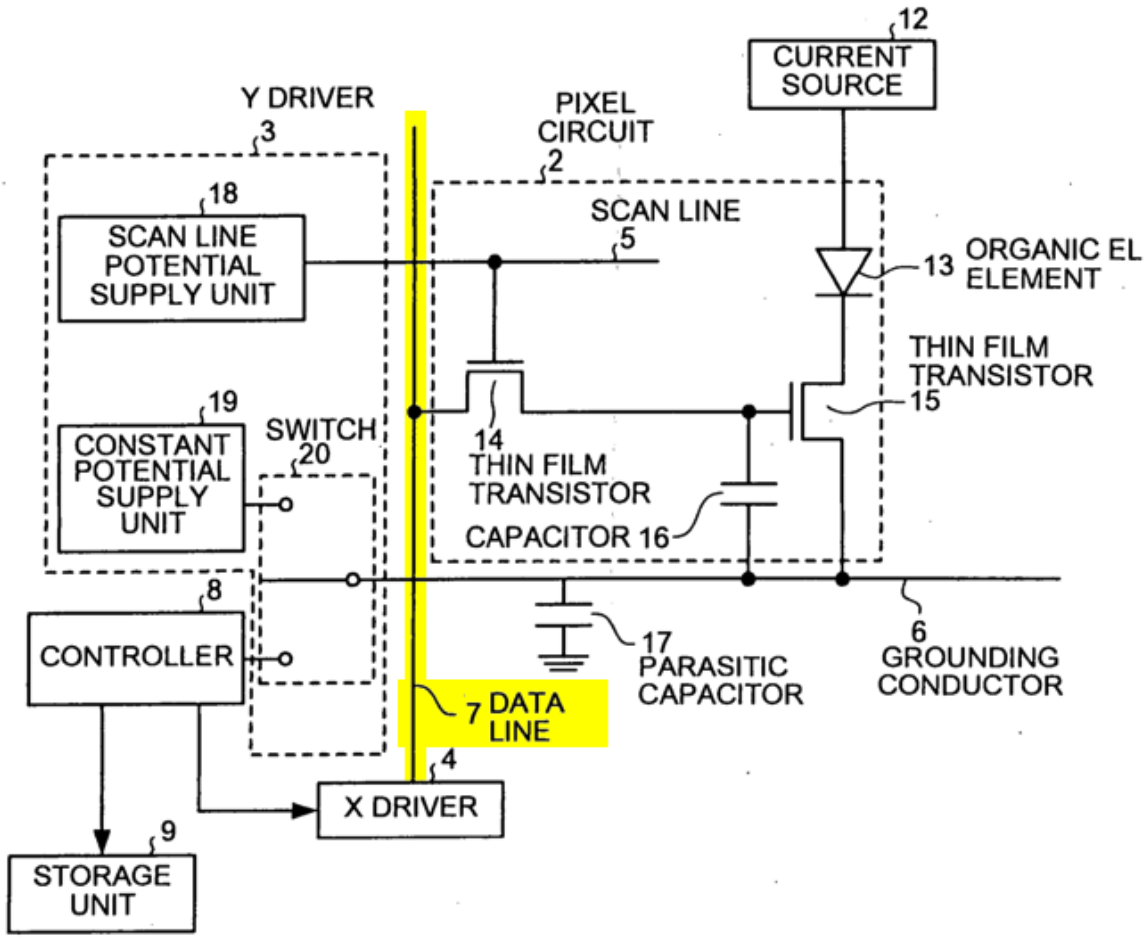
51. Prior to that amendment, a POSITA would have understood that the claims may have been intended to cover both types of gradation signals, voltages and currents, but not after. The applicants clarified this when they distinguished the prior art Ono reference as well. The applicants explained that Ono did not anticipate the claims because it "discloses applying a voltage by addition of a data voltage V_d and the threshold voltage V_{th} to the data line 7," and therefore "Ono et al does not disclose generating and supplying a gradation current as a gradation signal."

> It is respectfully submitted that, by contrast, Ono et al discloses a structure for deriving a threshold voltage V_{th} of a thin film transistor 15 based on a detection of a potential of a grounding line 6. In addition, Ono et al discloses applying a voltage obtained by addition of a data voltage V_D and the threshold voltage V_{th} to a data line 7.
>
> It is respectfully submitted that Ono et al does not disclose generating and supplying a gradation current as a gradation signal, in the manner of the gradation signal generation circuit of claim 1.

Ex. 7 ('137 File History) at 32 (August 24, 2010 Arguments Made in Amendment).

52. A POSITA would have found it immediately apparent that Ono is a voltage gradation circuit. For example, Figure 2 of Ono below shows the same circuit structure as in Figure 36 of the '137 patent where a voltage is provided on the data line to the gate of the drive transistor 15.

FIG.2



Ex. 6 (Ono) at Fig. 2

53. The prior art also confirms that POSITAs viewed generating a gradation current having a current as display data corresponding to a luminance gradation, as an ***alternative*** to generating a gradation voltage having a voltage value as display data corresponding to a luminance gradation. *See, e.g.*,

- "A data supplying method to pixels using the organic EL elements includes a voltage-programmed mode in which voltage-based data is supplied to data lines and a current-programmed mode in which current-based data is supplied to the data

lines." Ex. 21 (U.S. Patent No. 20050099412) at ¶ 4; *see also id.* at¶¶ 5, 6, Figs. 2, 5, 7, 17

- "In an AMOLED display there are transistors in each pixel circuit, and the programming of the pixels circuit to drive the desired current through the OLED is accomplished by applying a voltage to the transistors in the pixel circuit (for a voltage-programmed pixel), or by applying a current to the transistors in the pixel circuit (in a current-programmed pixel). Of course, the configuration of the transistors in the pixel will be different in the two cases." Ex. 22 (U.S. 2005/0067971) at ¶ 5; *see also id.* at ¶ 6 ("In a voltage-programmed display, the data applied to the data lines, i.e., columns, is a voltage, not a current").
- "The active matrix method is classified into a voltage programming method or a current programming method according to signal forms supplied for programming a voltage in the capacitor." Ex. 23 (U.S. Patent No. 7,501,999) at 1:40-2:40, Fig. 2.
- "The AMOLED displays are classified as either a voltage-programmed display or a current-programmed display. The voltage-programmed display is driven by a voltage-programmed scheme where data is applied to the display as a voltage. The current-programmed display is driven by a current-programmed scheme where data is applied to the display as a current." Ex. 24 (U.S. Patent No. 8,115,707).
- "[A] pixel of a conventional voltage-driven AMOLED…a gray scale to be displayed is determined by a voltage on a data line" Ex. 25 (U.S. patent No. 8,502,754) at 1:42-61; *see also id.* at 3:43-46 ("conventional current-driven AMOLED . . . The gray scale of the current-driven AMOLED pixel is determined by a magnitude of the current provided by the current source.").

- "The pixel circuit shown in Fig. 35 is different from that shown in Fig. 33. Luminance data is given in the form of voltage in the pixel circuit shown in Fig. 33, while the same data is given in the form of current in the pixel circuit shown in Fig. 35." Ex. 26 (U.S. Patent No. 7,015,882) at 1:45-3:38 (providing additional details), Figs. 33, 35.

54. In view of this well-known understanding in the art, a POSITA would have understood that a "gradation current having a current value" is an actual current with a value corresponding to a luminance level, and not a voltage with a value corresponding to a luminance level.

B. '891 patent

1. "a third thin film transistor which during driving its gate …" ('891 patent, claims 1, 3)

55. Claims 1 and 3 of the '891 patent each have a limitation "a third thin film transistor which during driving its gate through a driving conductor taps a diode driving current at an output of said first current-driving transistor and supplies a current measuring- and voltage regulating circuit, said current measuring- and voltage regulating circuit providing to the data conductor a voltage signal which is dependent on a current measuring result and a voltage comparison."

56. It is my opinion that a POSITA would have understood that the function of "providing to the data conductor a voltage signal" occurs during driving the third transistor's gate in view of the specification.

57. The specification supports that from the perspective of a POSITA, each of the claimed functions of tapping, supplying, and providing occur during driving the gate of the third transistor. For example, the specification states that in the "present invention" the third transistors gate is driven, and states that it "taps… and supplies…and provides."

> In keeping with these objects and with others which will become hereinafter, one feature of the present invention resides, briefly stated, in a driving circuit of the above mentioned general type, in which a third transistor is provided, which by driving its gate through a driving conductor taps the diode driving current at the output of the current-driving transistor and supplies a current measuring and voltage regulating circuit, and the current measuring-space and voltage regulating circuit provides to the data conductor a voltage signal which is dependent on current measurement results and a voltage comparison, wherein the driving of the gate of the third transistor acts due to its non-linear switching characteristic as a switch for a current deviation in the current measuring- and voltage regulating circuit.

'891 patent at 1:64-2:10.

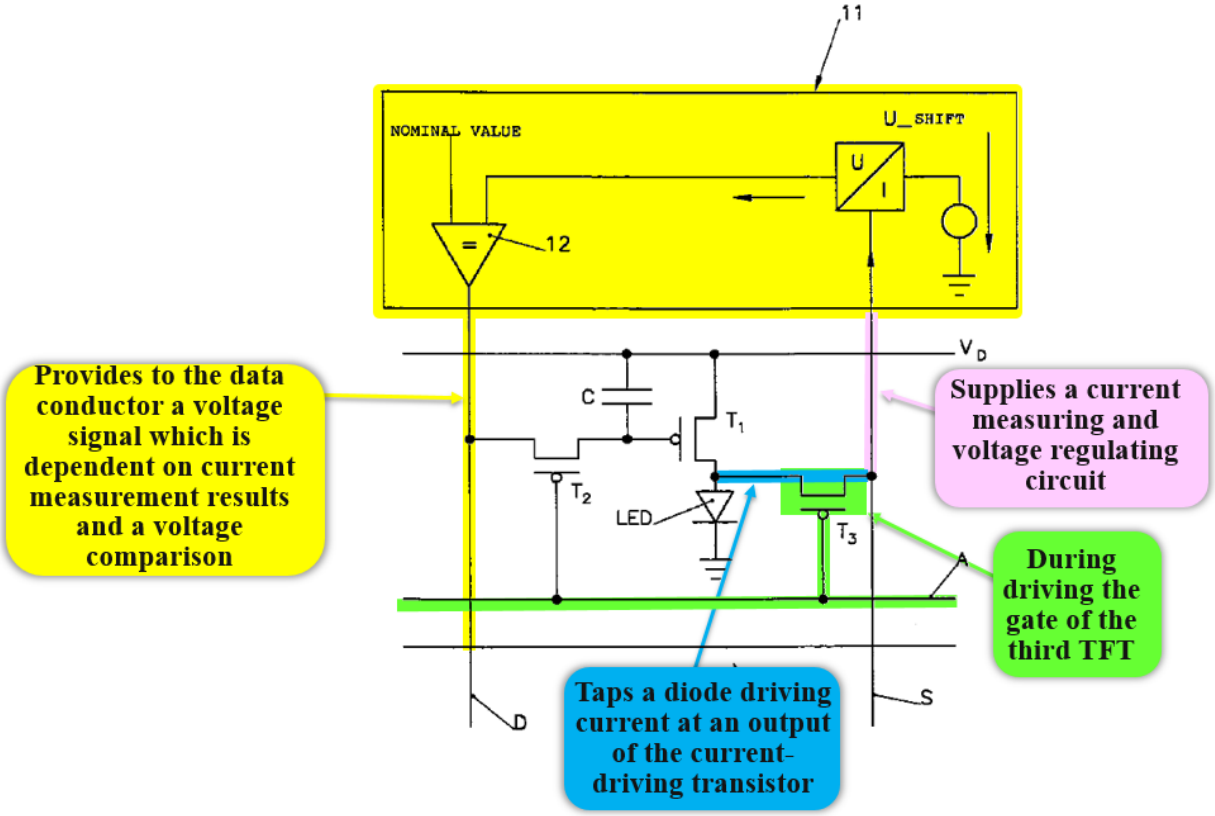
58. Similarly, the next paragraph in the specification states that "with this circuit," the circuit where the third transistors gate is driven, the "current to be measured is directly tapped," "[t]he measured value of the current is compared" and "in the case of deviation a corresponding correcting signal is provided at the input of the image point circuit."

> With this circuit the current to be measured is directly tapped at the output of the current-driving thin film transistor. The measured value of the current is compared with a nominal value, and in the case of deviation of the value a corresponding correcting signal is provided at the input of the image point circuit. Thereby after switching off of the third transistor, the driving current flowing through the LED is stabilized.

'891 patent at 2:11-18. A POSITA would have understood that the "input of the image point circuit" refers to the data conductor in the claim, and the "correcting signal" is the "voltage signal" that is provided to the data conductor in the claims. As shown above, the next sentence states that the third transistor is "switch[ed] off."

59. The sequential recitation of tapping, providing, and then turning off the transistor in this paragraph would have indicated to a POSITA that "providing" occurs while the transistor is switched on, which is while the gate is driven.

60. A POSITA also would have understood that the "providing" step occurs during driving the gate of the third transistor by analyzing the specification and the circuit diagram figure in the patent. To explain, below is an annotated version of the only disclosed Figure of the '891 patent, describing the different elements and their claimed functions (i.e., tapping, supplying, and providing) in the limitation beginning with "a third thin film transistor which during driving its gate." First, the diode driving current is tapped (blue) and flows through the third transistor (T3, light green) because its gate is driven. Second, the diode driving current is supplied (pink) to the "current measuring and voltage regulating circuit" (yellow) wherein "said current measuring and voltage regulating circuit" measures the current, compares the measured value with a voltage, and provides to the data conductor a voltage signal dependent on the current measurement and voltage comparison.



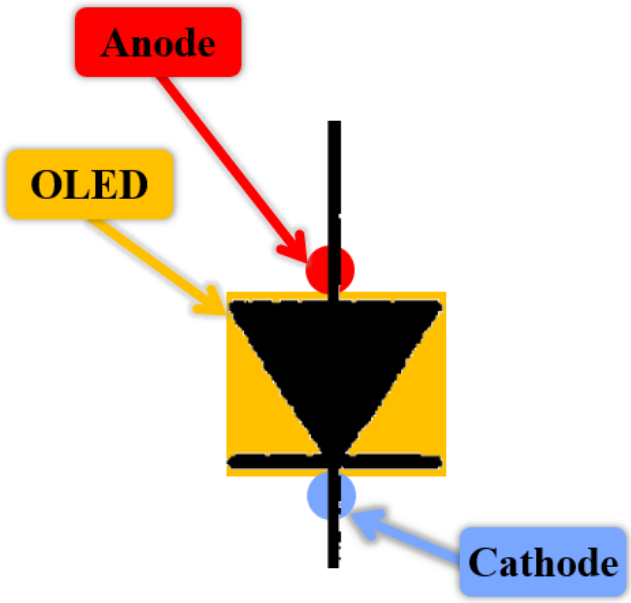
61. In this circuit, the "voltage signal" that is provided to the data conductor (D) is the input to the first current driving transistor (T1), which controls how much current is being tapped at the claimed "output of said first current-driving transistor," supplied to the current measuring and voltage regulating circuit (12), and measured (U/I). Accordingly, while the third transistor is driven, the output of the first current driving transistor is "fed back" to the input of the driving transistor as a voltage at the gate of T1. And each time the voltage at D changes, T1 will provide a different current value to be tapped, supplied and measured. This would happen continuously while the third TFT's gate is driven, allowing the drive current to be "regulated by the resistor [sic:transistor] T1 to the desired value." *Id.* at 3:9-21; *see also id.* at cls. 1, 3 (requiring "a feedback coupling"). In other words, while the third transistor is on, the diode driving current and voltage that is provided changes and then, when the third transistor is turned off, the current remains

constant. The ’891 patent confirms that this understanding is correct, as it states that only after the third transistor is “switched off,” the current “stabilizes.” *Id.* at 2:16-18.

2. “wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode” (’891 patent, claim 3)

62. The term “wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode” appears in claim 3 of the ’891 patent. In my opinion, a POSITA would have understood this to mean “wherein all above mentioned elements of the driving circuit are electrically connected to the anode or cathode of said light emitting diode.”

63. An OLED is like any diode, which is a circuit element that conducts current in one direction but not the other. The two “sides” of a diode are the anode side and the cathode side, and current flows from the anode to the cathode but not from the cathode to the anode. In a circuit diagram, a diode, including “organic light emitting” diodes, have the following schematic symbol that looks like an arrow pointing towards a straight line. The easiest way to remember which side is the anode and which is the cathode is that current can flow from the anode to the cathode, and so the direction the arrow is pointing is towards the cathode side.



64. In my opinion, the phrase "located at a same side" in the claims of the '891 patent refers to the electrical location, or electrical connection, of the drive circuit elements with respect to the light emitting diode in the circuit diagram of Figure 1.

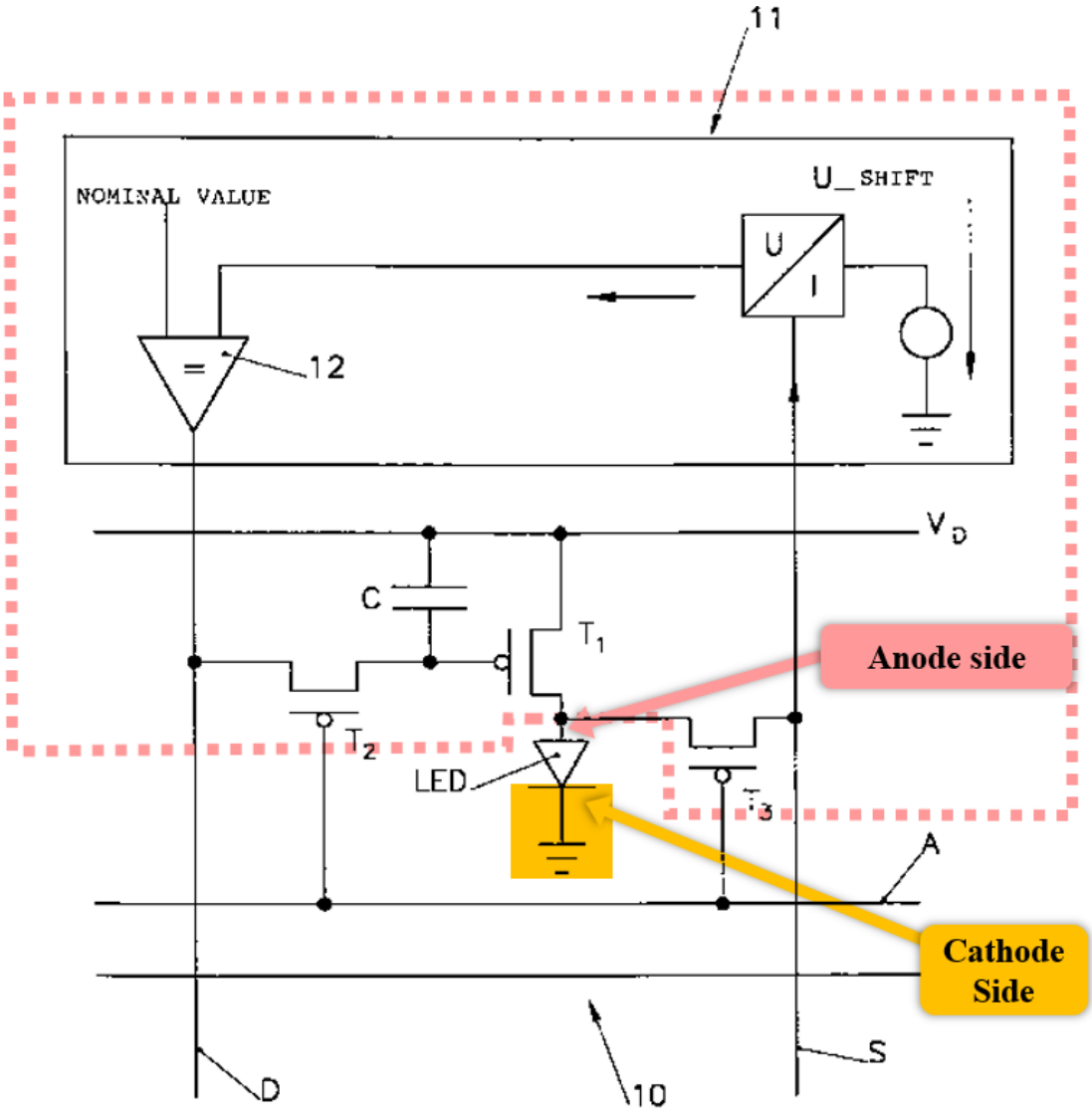
65. The prosecution history of the '891 patent supports that the "side" of the light emitting diode in claim 3 refers to the anode or cathode sides of the diode.

66. During prosecution, the applicant stated that claim 3's requirement that "all the above mentioned elements of the driving circuit are located at the same side of the light emitting diode" is "clearly shown in the drawings."

> The above mentioned features of the present invention are defined in claims 1 and 3. Claim 3 additionally defines that all the above mentioned elements of the driving circuit are located at the same side of the light emitting diode, so that no contacts must be guided through a semiconductor material of the diode. This is clearly shown in the drawings.

'891 FH at 127.

67. The '891 patent only includes a single "drawing," which is an electrical circuit diagram with common engineering symbols such as for an LED, transistors, and a capacitor. As shown below, it depicts "an organic, light-emitting diode LED with a cathode connected to ground" and the "circuit parts" are connected only to the "anode" side of the LED as shown in the annotated figure below. *Id.* at 2:25-27; *see id.* at 3:22-26 (referring to the "adjustable anode potential of the LED element"). A POSITA would understand that this Figure shows that all of the circuit elements are simply electrically located, i.e., electrically connected to the anode side of the LED.



'891 patent at Fig. 1.

68. This figure does not depict or disclose any shape, form, or geometry of a physical circuit, or of any physical "layer" or "layers" of the OLED. Nor is there any disclosure in the specification that describes the layers of material that make up the drive circuit elements as necessarily being physically oriented on one side or the other of the actually manufactured OLED device. Rather, the specification states that by electrically locating the elements on the same side of the circuit diagram, it would be possible to manufacture the circuit using a "conventional layer

sequence" and that it would not be "necessary" to use through contacting during manufacturing. '891 patent at 2:26-28. A POSITA would not have understood that the physical location of the drive circuit elements to be on the same side of any OLED layers would be required by the term "wherein all above mentioned elements of the driving circuit are located at a same side of said light emitting diode."

C. '068 patent

1. "formed on said plurality of supply lines along said plurality of supply lines" ('068 patent, claim 1) / "connected to said plurality of supply lines along said plurality of supply lines" ('068 patent at claim 13)

69. I understand that the term "formed on said plurality of supply lines along said plurality of supply lines" is found in Claim 1. Claim 1 recites:

> **1**. A transistor array substrate comprising:
> a substrate;
> a plurality of driving transistors which are arrayed in a matrix on the substrate, each of the driving transistors having a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain;
> a plurality of signal lines which are patterned together with the gates of said plurality of driving transistors and arrayed to run in a predetermined direction on the substrate;
> a plurality of supply lines which are patterned together with the sources and drains of said plurality of driving transistors and arrayed to cross said plurality of signal lines via the gate insulating film, one of the source and the drain of each of the driving transistors being electrically connected to one of the supply lines; and
> a plurality of feed interconnections which are formed on said plurality of supply lines along said plurality of supply lines, respectively.

70. I also understand that "connected to said plurality of supply lines along said plurality of supply lines" is found in Claim 13. Claim 13 recites:

13. A display panel comprising:
a substrate;
a plurality of driving transistors which are arrayed in a matrix on the substrate, each of the driving transistors having a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain;
a plurality of signal lines which are patterned together with the gates of said plurality of driving transistors and arrayed to run in a predetermined direction on the substrate;
a plurality of supply lines which are patterned together with the sources and drains of said plurality of driving transistors and arrayed to cross said plurality of signal lines via the gate insulating film, one of the source and the drain of each of driving transistors being electrically connected to one of the supply lines;
a plurality of feed interconnections which are connected to said plurality of supply lines along said plurality of supply lines;
a plurality of pixel electrodes each of which is electrically connected to the other of the source and the drain of a corresponding one of said plurality of driving transistors;
a plurality of light-emitting layers which are formed on said plurality of pixel electrodes, respectively; and
a counter electrode which covers said plurality of light-emitting layers.

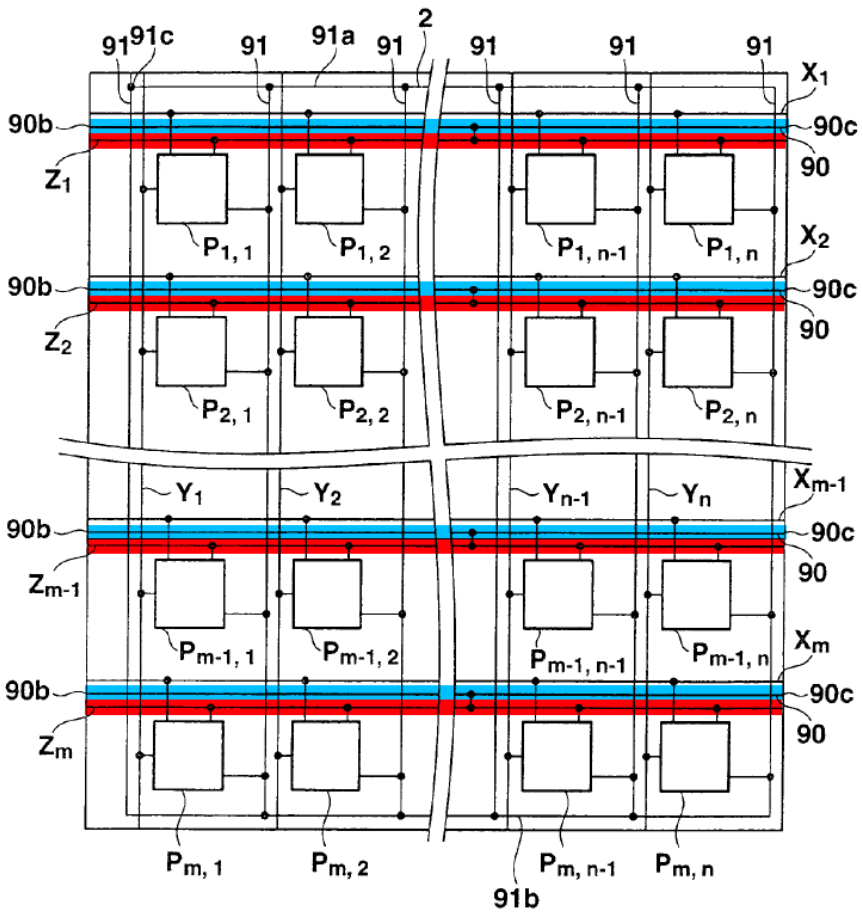
71. For the reasons discussed below, in my opinion, the meaning of "along said plurality of supply lines" is "over the length of said plurality of supply lines."

72. The term "along said plurality of supply lines" describes how the claimed "feed interconnections" are "formed on" (claim 1) or "connected to" (claim 13) the plurality of supply lines.

73. I'm not aware of "along" having any technical or scientific meaning in the art. As described below, the '068 patent uses the term "along" to have a non-technical meaning as reflected in dictionaries in the early 2000s. *See, e.g.*, Ex. 14 (The American Heritage College Dictionary (2002)) at p. 39 ("1. ***Over the length of***: walked along the path."); Ex. 15 (Webster's

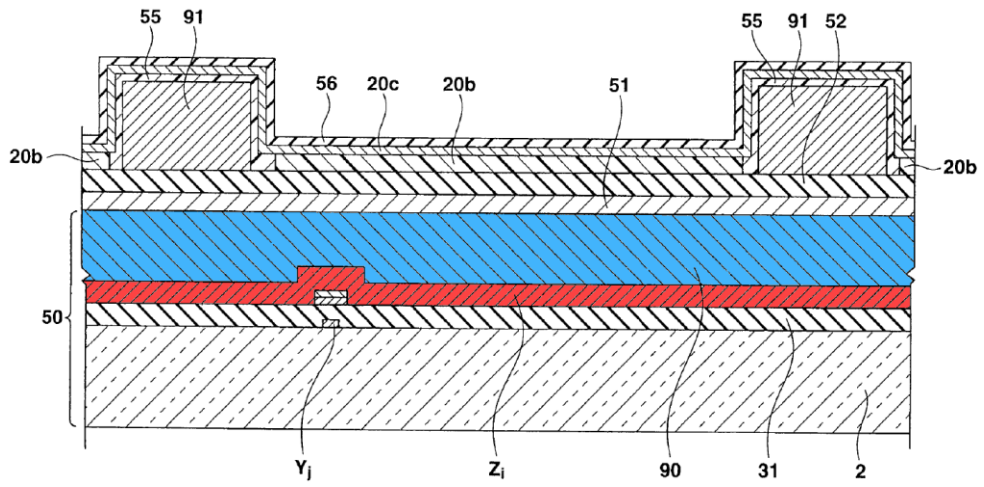
New World College Dictionary (2002)) at p. 40 ("1. On or beside the length of; ***over and throughout the length of*** [we hiked along the trail; along the driveway there is a hedge]"); Ex. 16 (Collins English Dictionary Complete and Unabridged) (2003)) at p. 45 ("1. ***Over or for the length of***, esp in a more or less horizontal plane: along the road").

74. The '068 patent describes two embodiments of its "feed interconnections." In the first embodiment, the specification discloses that the feed interconnections "are provided in parallel to the supply lines supply lines Z_1 to Z_m." '068 patent at 6:2-4. As shown below in Figure 1, which is a top view of the display panel, the supply lines (red) are arrayed horizontally across the display panel and connect to the pixels of a given row. The feed interconnections (blue) are similarly arrayed horizontally across the display panel in parallel with the supply lines. In this embodiment, each "feed interconnection" extends from one end of a respective "supply line" to the supply line's opposing end.



75. The specification discloses that the parallel structure in the first embodiment is achieved by first forming "a plurality of long trenches 34 (FIG. 8) running in the horizontal direction ***along the supply lines Z1 to Zm.***" *Id.* at 10:17-20. Next, the feed interconnections are buried in these trenches and "formed on the upper surface of the supply lines Z to Z_m to be electrically connected to them." *Id.* at 6:33-35, 10:23-29.

76. A side view of this embodiment is shown below in Figure 6, wherein the feed interconnections (blue) are formed on the upper surface of the supply lines (red) and extend parallel to the supply lines in the horizontal direction.



77. In this embodiment, the specification further discloses that "conductive lines" are formed on the feed interconnections along them. *Id.* 11:7-11. Specifically, the specification discloses that "on the feed interconnections 90 . . . conductive lines 51 ***electrically connected to the feed interconnections 90 along them*** are patterned." *Id.* A side view of this embodiment is depicted in Figure 6, which shows the conductive lines 51 (yellow) are formed on the upper surface of the feed interconnections (blue) and extend across the length of the feed interconnections in the horizontal direction.

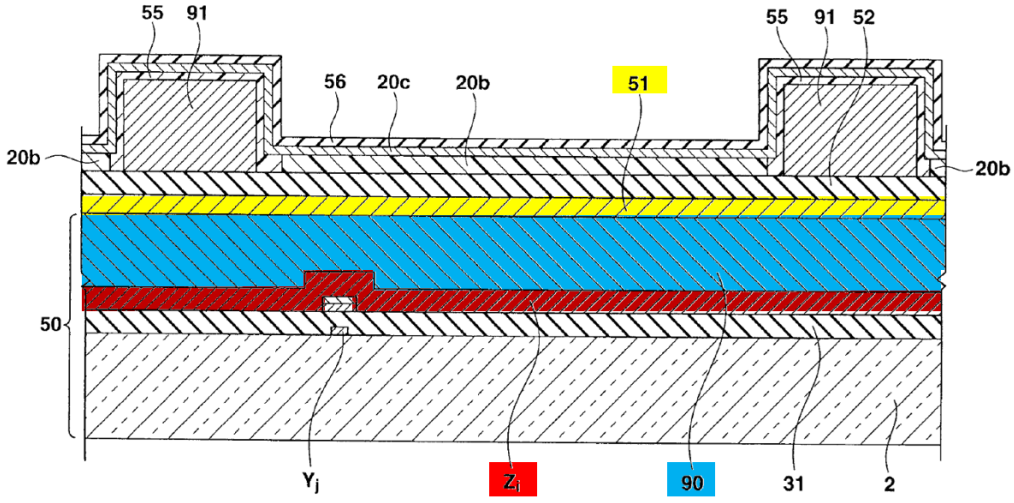
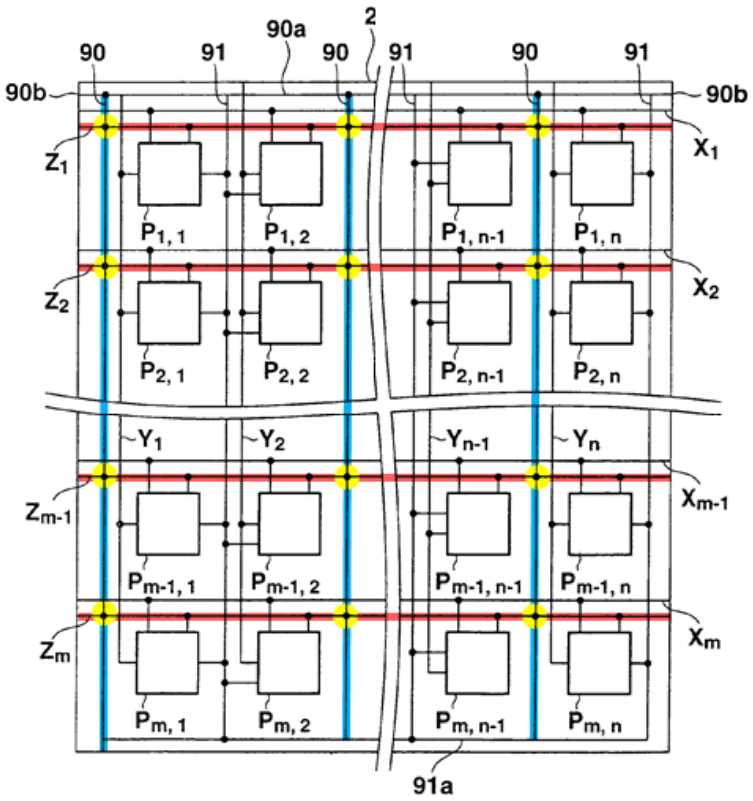


FIG.6

78. In the second embodiment, shown in Figure 20 below, "[t]he feed interconnections 90 are connected to the supply lines Z_1 to Z_m, and branched in parallel to the signal lines Y_1 to Y_m, when viewed from the upper side." *Id.* at 23:1-3. In this embodiment, each "feed interconnection" (blue) is connected to each "supply line" (red) such that it forms a grid. In this grid configuration, each supply line has connections (yellow) to the "plurality of feed interconnections" over the horizontal length of the supply line. *Id.* at 27:6-11. The connections (yellow) between the feed interconnections and the supply lines are "along" the supply lines.



79. To a POSITA, each of these Figures supports that the "feed interconnections" are formed on or connected to the supply lines over the length of the supply lines.

80. The purpose of the "feed interconnections," and the problem the '068 patent was trying to solve, also would have informed a POSITA that "along" is used in the claims to mean "over the length of." The patent discloses that the intended purpose of the invention is to

"satisfactorily drive a light-emitting element while suppressing any voltage drop and signal delay.". '068 patent at 2:39-41, 3:60-4:14.

81. As explained in the Background of the Invention, driving circuits include "interconnections such as a power supply line to supply a current to an organic EL element," which "are patterned simultaneously in the thin film transistor patterning step by using the material of a thin-film transistor such as a switching transistor or driving transistor." '068 patent at 1:57-62; *see also id.* at 1:62-2:9. The '068 patent, however, recognizes that a problem occurs when supply lines are patterned together with the TFT electrodes (gates, sources and drains) because TFT electrodes are designed to be thin—hence the name ***thin-film*** transistors. *Id.* Accordingly, when supply lines are patterned together with the thin-film electrodes, as was conventional, the same thin-film is used both for the electrodes and the supply lines meaning the supply lines are thin as well. *Id.* Because of this, the '068 patent states that the supply line has a high resistance and the necessary amount of current cannot be provided through the supply line to the organic EL elements along it. *Id.* at 2:9-14; 18:26-30 ("The resistance of a thin film such as the gate or the source/drain of a thin-film transistor is so high that the write current (i.e. driving current) cannot be supplied to the organic EL elements 20.").

82. To provide additional context, "supply lines" are designed to provide current to a "plurality of light-emitting elements." '068 patent at 2:8-11. For example, the supply lines will be arrayed across a display panel in a direction, such that each supply line can supply current to illuminate the pixels arranged in that direction across the display. *See, e.g.*, '068 at Figs. 1, 20, 5:60-67; 6:7-11; 22:50-65; 23:35-39. In the '068 patent, the supply lines (red) are arrayed horizontally across the display to supply current to illuminate the pixels (yellow) in the corresponding row.

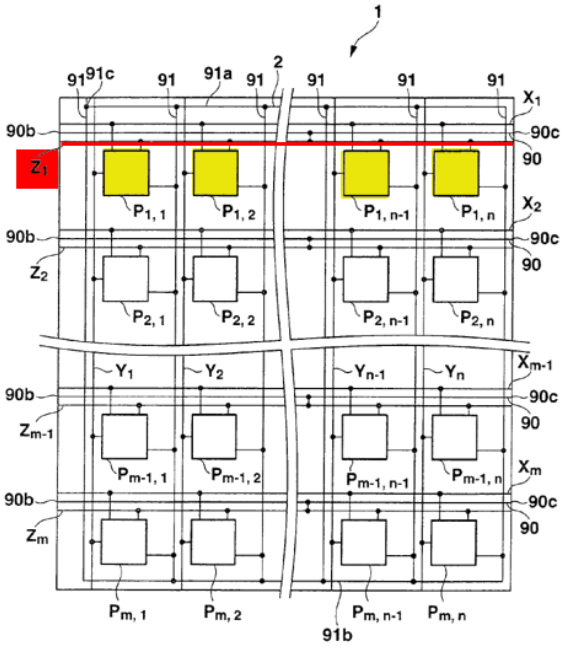


FIG.1

'068 patent Fig. 1.

83. The resistance of a conductor is equal to the length of the conductor between two points, times the "resistivity" of the metal, divided by the cross sectional area of the conductor (width times thickness). The resistivity of a conductor is generally constant (that is dependent on the material used), so the longer a line is the greater its resistance, and the greater the cross sectional area (i.e., width times thickness) the less its resistance. *See* '068 patent at 20:51-22:44 (discussing resistivity, length, and sectional area of feed interconnections).

84. The '068 patent explains that the high resistance of a thin supply line leads to two problems when supplying the current to a plurality of pixels through it: "voltage drop" or "current flow through the interconnection delays" (also referred to as "signal delays"). *Id.* at 2:5-14. In order to suppress these problems, "the resistance of the interconnection is preferably low." *Id.* at 2:12-14. Although, the '068 patent notes that it is possible to reduce the resistance of the supply line interconnection in the metal layer serving as the source and drain of the TFT, or the metal layer serving as the gate of the TFT (collectively, "TFT layers" or "TFT electrodes"), such as by

making the supply line thicker or wider, it expressly discourages it. *Id.* at 2:14-35. For example, the ’068 patent explains that using the TFT layers to reduce resistance creates more problems, such as increased parasitic capacitance that “retards the flow of the current,” decreases in “the ratio of the light emission area,” “large changes in transistor characteristics,” decreases in “etching accuracy,” and adverse effects of transistor characteristics. *Id*.

85. Accordingly, to decrease the voltage drop and signal delay problems in the supply lines formed in the TFT layers, the ’068 patent discloses that separate conductive structures, called “feed interconnections,” are “stacked on the supply lines and formed separately for [sic:from] the drains, sources, and gates of the driving transistor.” ’068 patent at 3:61-4.3. This allows the feed interconnections to be made thicker than the TFT layers with a reduced resistance and, because they are stacked on the supply lines over the length of them, the feed interconnections help to share the flow of current as it is supplied to each of the light emitting elements along the supply line. *Id.* at 3:61-4:14, 10:25-32, 18:26-40, 26:62-66. This has the effect of reducing the resistance of the path for current to flow to the pixels through the supply lines. *Id.* For this reason, the feed interconnections in both embodiments are over the length of the supply lines, so that they can reduce the resistance of the supply lines across the pixel area in the display panel. *Id.* at Figs. 1, 6, 20, 25; *see id.* at 20:25-33 (“total length of the feed interconnection” extends across 1366 pixels in the row direction). In the first embodiment, the feed interconnections reduce the resistance of the supply lines by increasing the effective cross sectional area of the line. *Id.* at 6:2-4, 10:17-33, 18:26-40. In the second embodiment, the feed interconnections reduce the resistance of the supply lines over the length of the supply line by decreasing the effective length of the supply line that current travels. *Id.* at 23:1-3, 26:62-66.

86. This problem and solution is reflected in the claim language, which requires that the supply lines are patterned with the sources and drains of the drive transistor. '068 at claims 1, 13 (requiring "plurality of supply lines which are patterned together with the sources and drains"). Thus, as taught by the '068 patent and as a POSITA would understand, the claimed supply lines would be formed thin and have too high of a resistance to provide sufficient current to a plurality of light emitting elements. '068 patent at 1:57-2:12, 18:26-30 ("The resistance of a thin film such as the gate or the source/drain of a thin-film transistor is so high that the write current (i.e. driving current) cannot be supplied to the organic EL elements 20."). And in each claim, the "feed interconnections" are formed or connected to the supply lines ***along*** the supply lines, so that the feed interconnections can decrease the resistance of the supply lines as discussed above.

87. A POSITA would not have understood "along" to mean "at a point" as it would defeat the purpose of the alleged invention. Specifically, if a feed interconnection is only connected at a single point on a supply line, the feed interconnection would not improve voltage drop or signal delay problems because the resistance of the supply line would remain the same. The supply lines effective cross sectional area would not be increased over its length, nor would there be a decrease in the length for current to flow through the supply line. In particular, a feed interconnection that only connects to the supply lines at a single point would not address the voltage drop and signal delay problem that occurs particularly for pixels furthest from that point of connection.

88. Thus, it is my opinion that "along said plurality of supply lines" means "over the length of said plurality of supply lines."

2. "patterned together" (Claims 1 and 13)

89. The terms "patterned" and "patterned together" are found in Claim 1 and Claim 13. Claim 1 recites:

1. A transistor array substrate comprising:
a substrate;
a plurality of driving transistors which are arrayed in a matrix on the substrate, each of the driving transistors having a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain;
a plurality of signal lines which are patterned together with the gates of said plurality of driving transistors and arrayed to run in a predetermined direction on the substrate;
a plurality of supply lines which are patterned together with the sources and drains of said plurality of driving transistors and arrayed to cross said plurality of signal lines via the gate insulating film, one of the source and the drain of each of the driving transistors being electrically connected to one of the supply lines; and
a plurality of feed interconnections which are formed on said plurality of supply lines along said plurality of supply lines, respectively.

90. Claim 13 recites:

13. A display panel comprising:
a substrate;
a plurality of driving transistors which are arrayed in a matrix on the substrate, each of the driving transistors having a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain;
a plurality of signal lines which are patterned together with the gates of said plurality of driving transistors and arrayed to run in a predetermined direction on the substrate;
a plurality of supply lines which are patterned together with the sources and drains of said plurality of driving transistors and arrayed to cross said plurality of signal lines via the gate insulating film, one of the source and the drain of each of driving transistors being electrically connected to one of the supply lines;
a plurality of feed interconnections which are connected to said plurality of supply lines along said plurality of supply lines;
a plurality of pixel electrodes each of which is electrically connected to the other of the source and the drain of a corresponding one of said plurality of driving transistors;
a plurality of light-emitting layers which are formed on said plurality of pixel electrodes, respectively; and
a counter electrode which covers said plurality of light-emitting layers.

91. Claims 1 and 13 thus include the same two "patterned" requirements: (1) "a plurality of signal lines which are ***patterned together*** with the gates of said plurality of driving transistors" and (2) "a plurality of supply lines which are ***patterned together*** with the sources and drains of said plurality of driving transistors."

92. For the reasons discussed below, the meaning of "patterned" is "formed of the same layer" and "patterned together" is "patterned at the same time."

93. The '068 patent uses the term "patterned" to describe "manufacturing the display panel," which is an integrated circuit comprising transistors, capacitors, organic light emitting diodes, and conductive lines. '068 patent at 1:63-2:4, 14:17-15:40 (section entitled "Manufacturing Method of Transistor Array Substrate and EL Display Panel"). The specification discloses that the components and lines of the display panel are formed by overlaying different

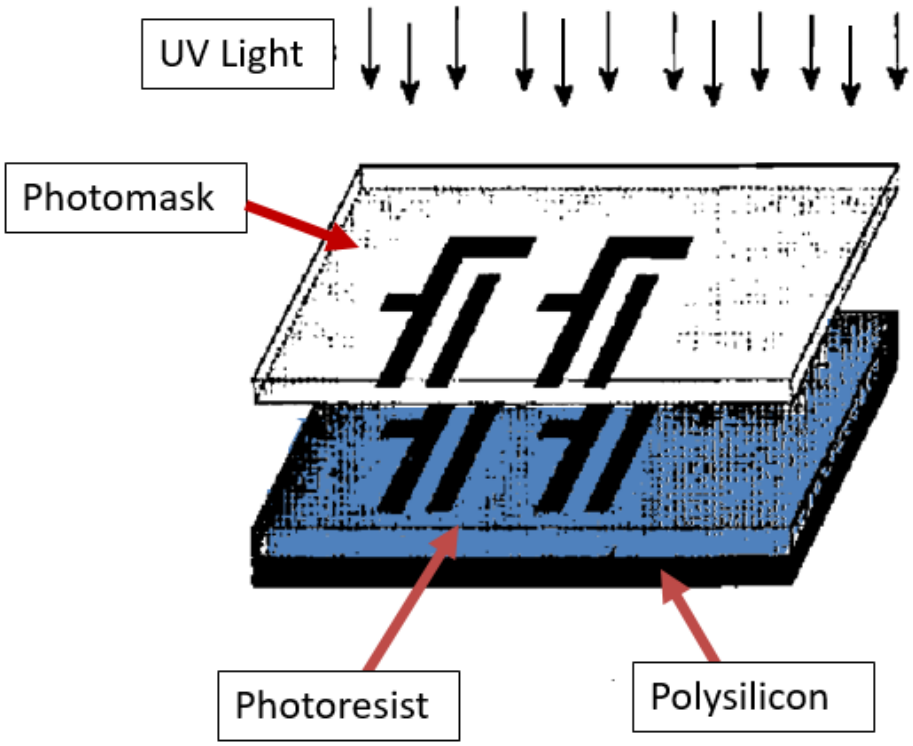
layers one by one using three well-known semiconductor manufacturing processes: "deposition," "photolithography," and "etching."

94. In this context, patterning has a well-known meaning to those of ordinary skill in the art. As I explained in my textbook, published in 2002, "[a]ll integrated circuits consist of various layers that overlay [each other] to form the device or component," wherein "each distinct layer must be defined as a collection of geometries." Ex. 19 (CMOS) at 23. Each integrated circuit begins with a starting material, called a substrate, and then the well-known semiconductor manufacturing techniques of "deposition," "photolithography," and "etching" are sequentially executed to manufacture the relevant semiconductor components and lines. *See, e.g.,* Ex. 19 (CMOS) at 23-24, Fig. 2.1-4.

95. The first step, deposition, comprises depositing a layer of material across the entire surface of the substrate. This can be achieved by a variety of deposition methods, including vapor deposition such as physical vapor deposition (PVD) or chemical vapor deposition (CVD).

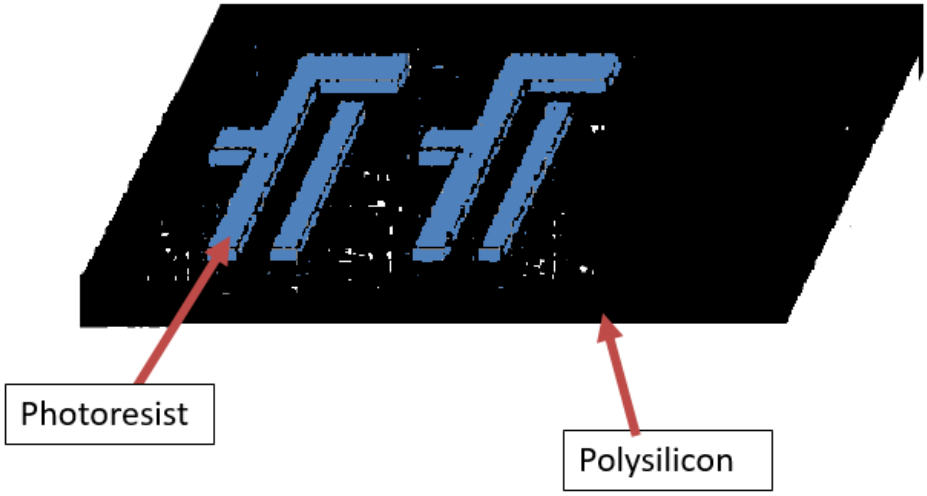
96. The second step, photolithography, comprises creating a "mask" for transferring a desired pattern to the deposited layer using ultraviolet light (UV light). During photolithography, a "photoresist" is deposited on the surface of the layer to be patterned. Because the characteristics of the photoresist change when exposed to UV light, one can use the photoresist to transfer a pattern from a photomask to the deposited layer by selectively exposing areas of the layer to UV light.

97. For example, as shown below in annotated Figure 2.1-4, a photomask is created with the desired pattern to be transferred to the layer, much like a stencil. A photoresist (blue) is deposited on the desired layer to be patterned, here the polysilicon (black). Next, one uses the mask to selectively expose the photoresist on the layer to UV light.



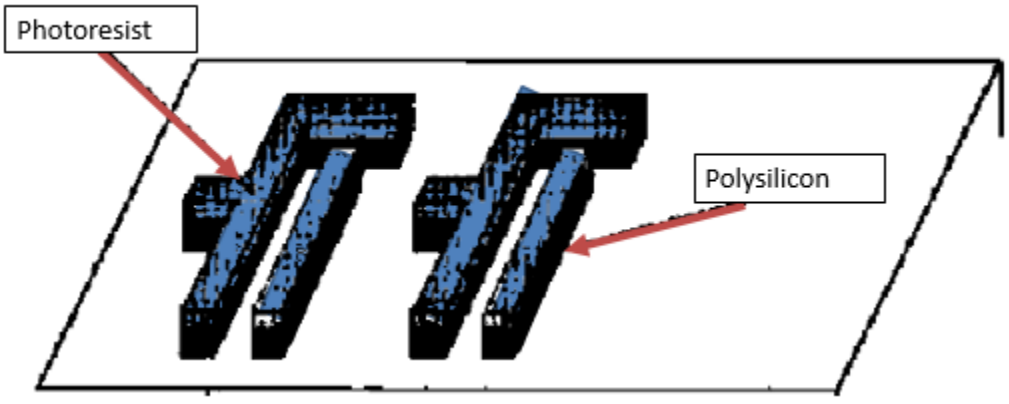
Ex. 19 at 24 Fig. 2.1-4(a) (annotated, cropped).

98. Using the type of mask shown in the example above, the areas exposed to UV light (material below the white regions of the mask) will be removed, and the areas that were not exposed to UV light (area beneath the black pattern of the mask) will remain. Ex. 19 (CMOS) at 24. As shown below in annotated Figure 2.1-4, the only photoresist (blue) that remains on the polysilicon (black) is the portion that was not exposed to the UV light.



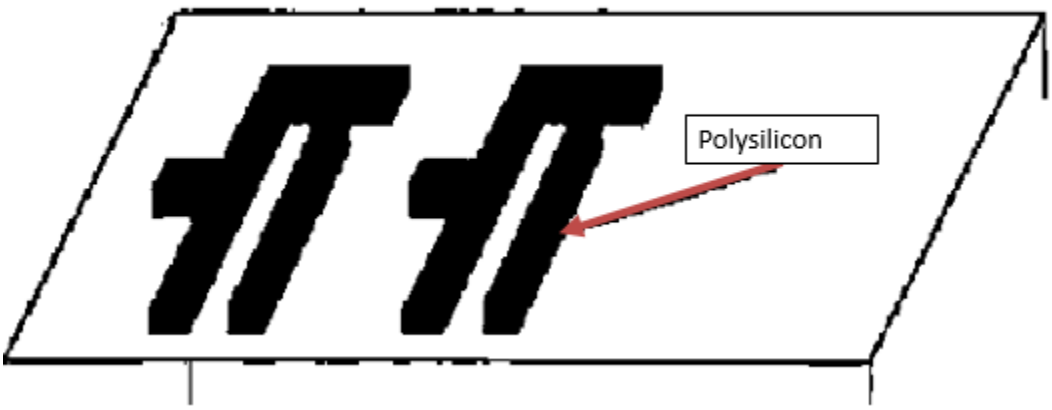
Ex. 19 at 24 Fig. 2.1-4 (b) (annotated, cropped).

99. Next, one etches the desired layer to be patterned—here the polysilicon—to remove the portions of the deposited layer that are unprotected by the mask. Specifically, the remaining photoresist protects selected areas of polysilicon from being removed by the etch plasma or acids. As shown below in annotated Figure 2.1-4, the only polysilicon (black) remaining is that underneath the photoresist (blue).



Ex. 19 at 24 Fig. 2.1-4(c) (annotated, cropped).

100. Once the etching process is complete, the photoresist is removed without damaging the underlying polysilicon layer. The resulting polysilicon layer (black) reflects the desired pattern from the original photomask.



Ex. 19 at 24 Fig. 2.1-4(d) (annotated).

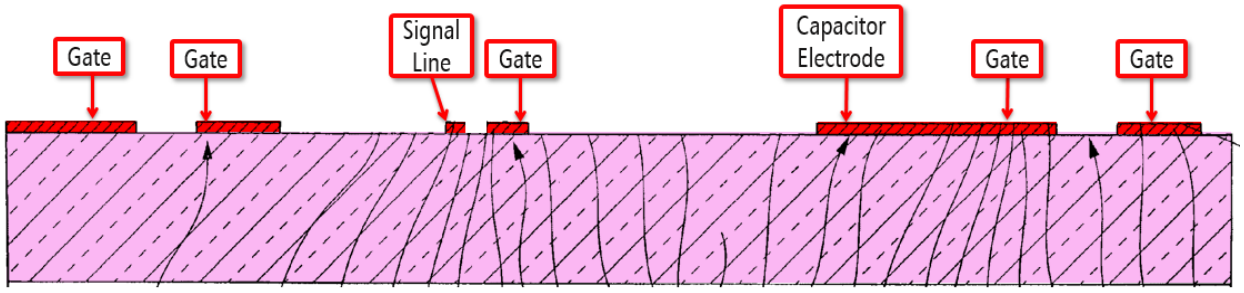
101. As I explained in my textbook, "[t]his process must be repeated for each layer of the integrated circuit." Ex. 19 (CMOS) at 24.

102. The components or lines in each layer are formed at same time because the depositing, photolithography, and etching steps are performed sequentially to the entire layer. Thus, if two components are formed in the same layer, both components will be formed during the same deposition, photolithography, and etching steps.

103. The specification of the '068 patent discloses manufacturing the display panel in a manner consistent with the well-known patterning process discussed above.

104. For example, the specification discloses that first a gate layer is formed on the base insulating substrate. The gate layer is formed on the substrate by depositing a material onto the substrate through "vapor deposition such as CVD, PVD, or sputtering." '068 patent at 14:22-24. The gate layer is then "sequentially subjected to photolithography and etching to pattern the gates

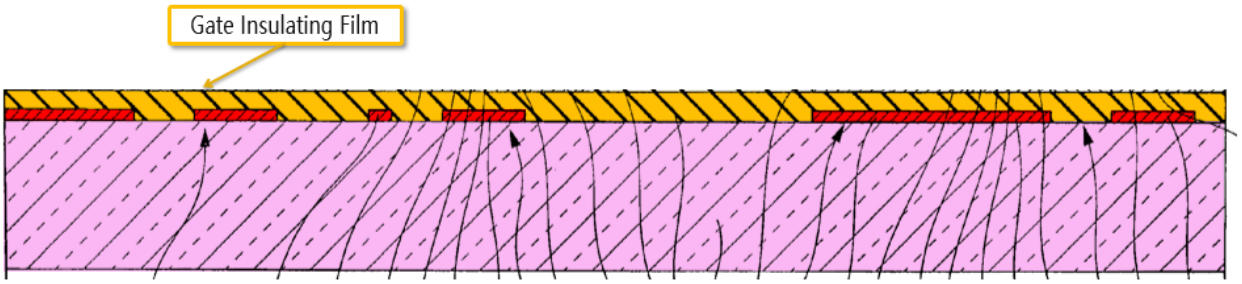
21g, 22g, and 23g, and the electrodes 24A of the pixel circuits P_{ij} to P_{mn}, and the signal lines." *Id.* at 14:24-27. A side view of the completed gate layer is shown in annotated and cropped Figure 5 below wherein the gate layer (red) is formed on the insulating substrate (pink).



'068 patent at Fig. 5 (annotated, cropped).

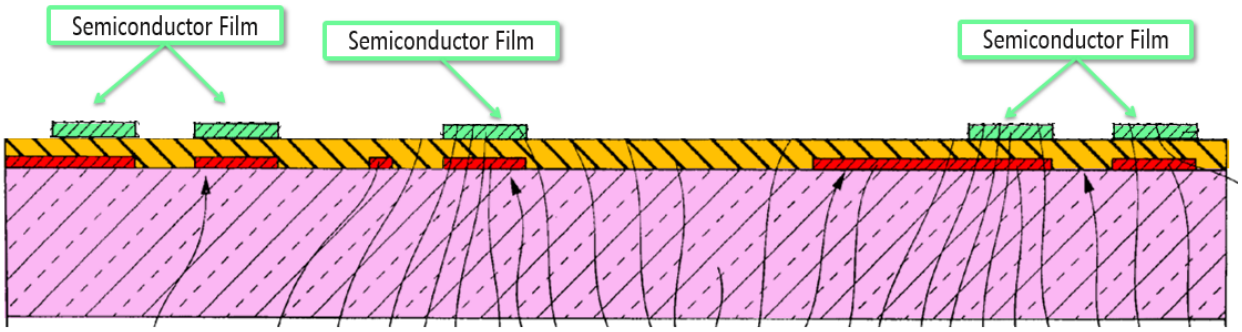
105. As shown in the above Figure 5, above, all components in the gate layer—the signal lines, gates, and capacitor electrodes—are formed from a single layer. The specification confirms this understanding by disclosing to a POSITA that the signal lines, gates, and capacitor electrodes "are formed, using photolithography and etching, by ***patterning a single conductive film***." '068 patent at 9:18-28. A person of ordinary skill would further understand that the signal lines, gates, and capacitor electrodes were patterned at the same time because they are formed using the same deposition, photolithography, and etching steps. *See, e.g., id.* at 25:4-10 (the "gates" of the TFTs and the "signal lines … are ***simultaneously formed***, using photolithography and etching, by patterning a conductive film.").

106. Next, the specification discloses the formation of the gate insulating film. The specification discloses that the gate insulting film is formed on the surface of the gate layer by "vapor deposition." '068 patent at 14:28-31. Then, contact holes, which are holes formed in an insulating layer such that opposing layers can be connected, are formed by "photolithography and etching." *Id.* A side view of the completed gate insulating film is shown in annotated and cropped Figure 5 below wherein the gate insulating film (orange) is formed on the gate layer (red).



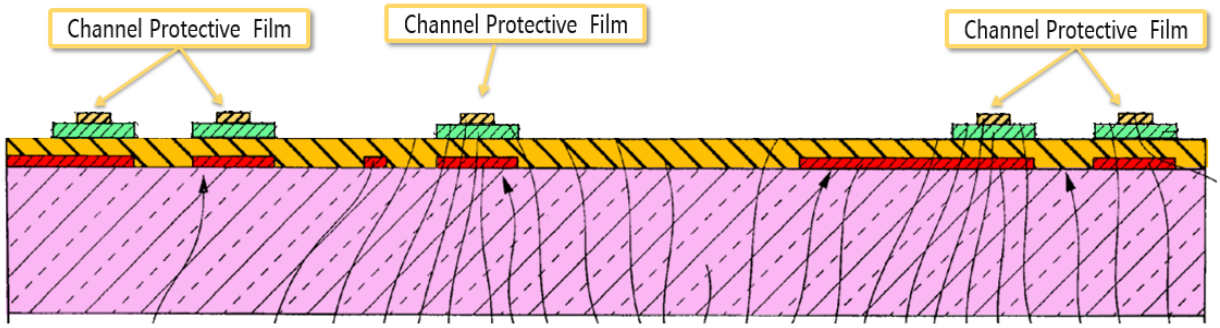
'068 patent at Fig. 5 (annotated, cropped).

107. Next, semiconductor films is patterned on the gate insulating. The patent discloses depositing a layer through vapor deposition. *Id*. at 14:32-34. The semiconductor film is then patterned using photolithography and etching. *Id.* A side view of the completed semiconductor film is shown in annotated and cropped Figure 5 below wherein the semiconductor film (green) is formed on the gate insulating film (orange).



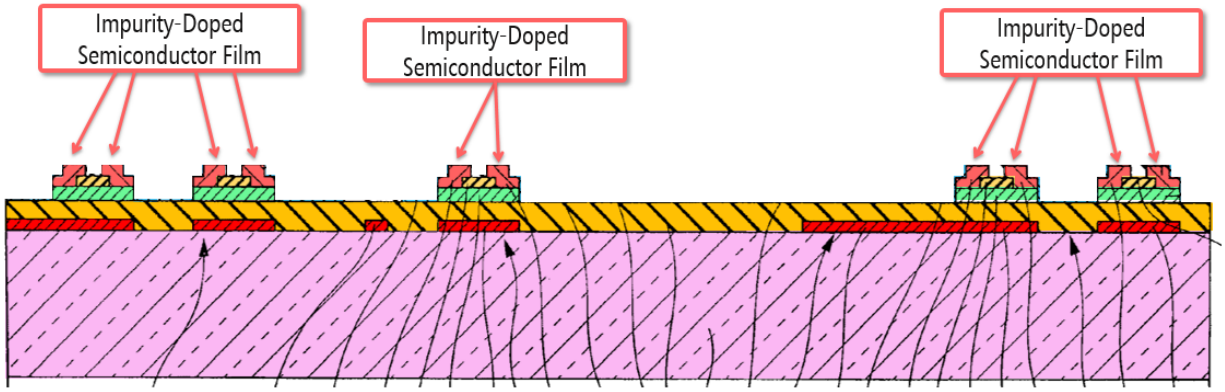
'068 patent at Fig. 5 (annotated, cropped).

108. The channel protective film is next patterned on the semiconductor films by sequentially executing vapor deposition, photolithography, and etching. *Id*. at 14:34-37. A side view of the completed channel protective film is shown in annotated and cropped Figure 5 below wherein the channel protective film (yellow) are formed on the semiconductor film (green).



'068 patent at Fig. 5 (annotated, cropped).

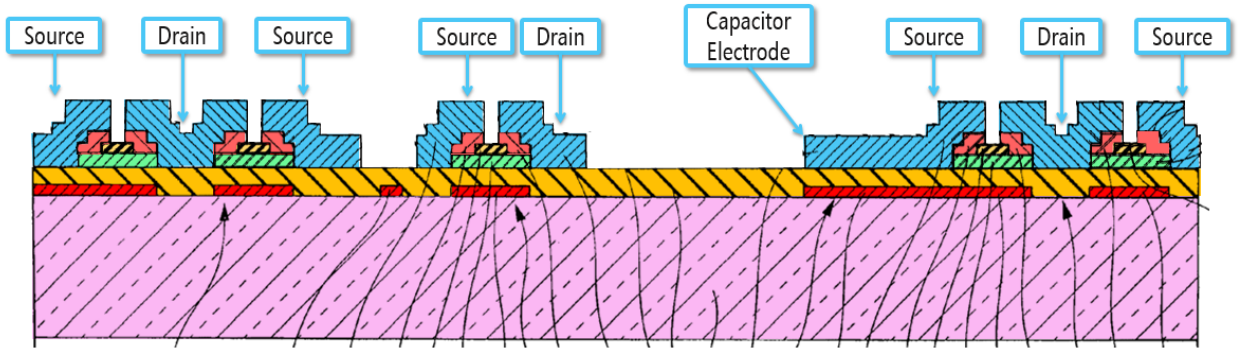
109. The patent discloses that the impurity-doped semiconductor film is patterned next by sequentially executing vapor deposition, photolithography, and etching. *Id.* at 14:37-41. A side view of the completed impurity doped semiconductor film is shown in annotated and cropped Figure 5 below wherein the impurity-doped semiconductor film (dark pink) is formed on the channel protective film (yellow) and the semiconductor film (green).



'068 patent at Fig. 5 (annotated, cropped).

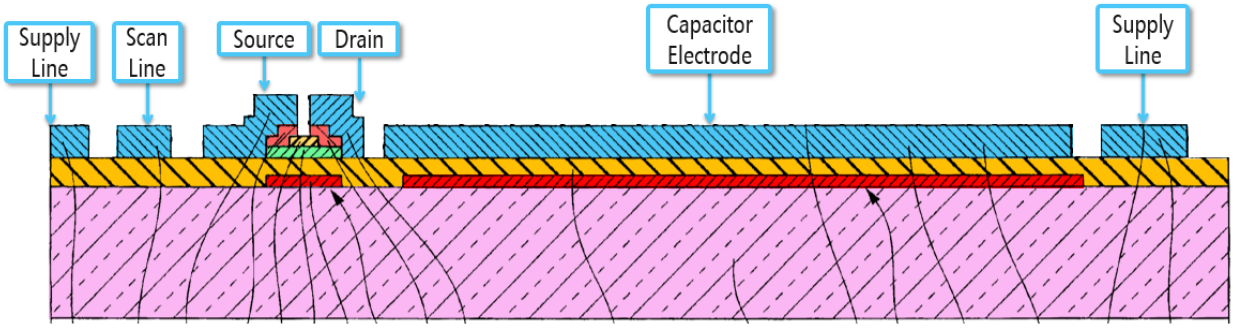
110. Next, the specification discloses forming the drain layer. First, a layer is deposited across the surface of the existing substrate. *Id.* at 14:42-45 The layer is then "sequentially subjected to photolithography and etching to pattern" the drains, sources, pixel electrodes 24B, the scan lines, and the supply lines. *Id.* at 14:46-50. A side view of the completed drain layer is shown

in annotated and cropped Figure 5 below wherein the drain layer (blue) is formed on the gate insulating layer (orange) and the impurity doped semiconductor films (dark pink)



'068 patent at Fig. 5 (annotated, cropped).

111. Another side view of the completed drain layer is shown in annotated and cropped Figure 8 below wherein the drain layer (blue) is formed on the gate insulating layer (orange) and the impurity doped semiconductor films (dark pink).

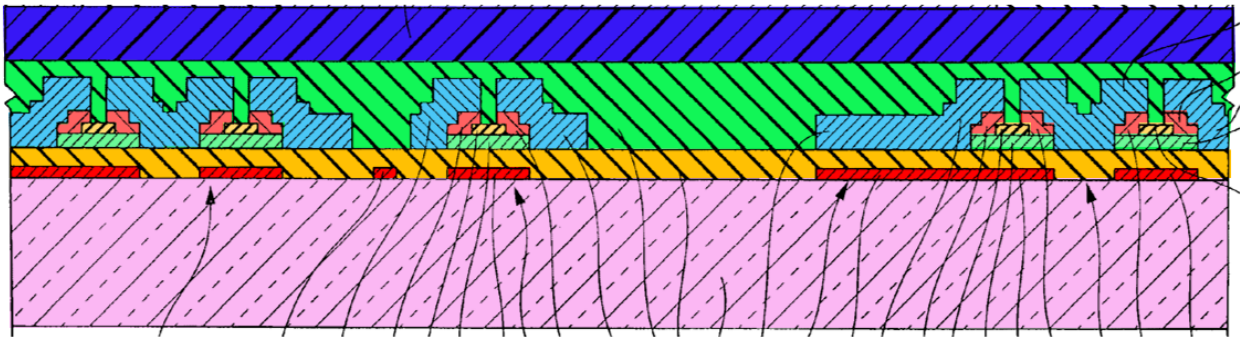


'068 patent at Fig. 5 (annotated, cropped).

112. As shown in Figure 5 and Figure 8 above, all components in the drain layer—the sources and drains, supply lines, scan lines, and capacitor electrodes 24B—are formed in a single layer. The specification confirms this understanding, stating "the drains 23d and sources 23s of the driving transistors 23 … and the supply lines Z_1 to Z_m are formed, using photolithography and etching, by ***patterning a single conductive film***." '068 patent at 9:36-51; *see also* 9:2-4 ("The drains 21d to 23d and source 21s to 23s of the transistors 21 or [sic] 23 are formed by ***patterning***

the same material layer."), *Id.* at 25:4-10. A person of ordinary skill would further understand that the supply lines, sources and drains, scan lines, and capacitor electrodes are patterned at the same time because they are formed using the same deposition, photolithography, and etching steps.

113. The specification then discloses depositing a "protective insulating film" on the drain layer. *Id.* at 14:51-52. A coating is then applied to the protective insulating film to form the "planarization film." *Id.* at 14:52-54. A side view of the completed transistor substrate with the protective insulating film (bright green) and planarization film (dark blue) is shown in annotated and cropped Figure 5 below.



'068 patent at Fig. 5 (annotated, cropped).

114. Similar layered structures are shown in the rest of the '068 patent's figures as well. *See, e.g.,* '068 patent at Figs. 5-11, 22-25; *see also id.* at 11:11-14, 26:40-43 (describing "conductive lines 51 are patterned together with the pixel electrodes 20a by etching a conductive film"), Fig. 8 (showing conductive lines 51 and pixel electrodes 20a in the same patterned layer). Thus, it's clear to a POSITA that the '068 patent uses "patterned" to describe the formation of the display panel layer by layer, consistent with its ordinary usage in the art. It is my opinion that "patterned" means "formed in a single layer" and "patterned together" means "patterned at the same time."

115. I understand that Solas would construe "patterned" and "patterned together" as "formed in one or more layers" and "formed to fit together." This does not reflect how the terms would be understood by a POSITA in view of the evidence above. Patterning is a well understood process that must be repeated for each layer, which is how the term is used in the '068 patent. The '068 patent only refers to patterning components as part of a single layer, and does not refer to components formed in different layers as being "patterned" or "patterned together." I have also reviewed the '068 patent and its file history, and there is no disclosure of the term "to fit" or the concept of "fitting," as Solas proposes in its construction of "patterned together." Thus, a POSITA would not have understood "patterned together" to mean "patterned to fit together," and would not understand what "to fit" means in the context of the '068 patent.

3. "feed interconnections" (Claims 1, 10, 12, 13, 17)

116. The term "feed interconnections" is found in independent claims 1 and 13 and dependent claims 10, 12, 13, and 17. Claim 1 recites:

> **1**. A transistor array substrate comprising:
> a substrate;
> a plurality of driving transistors which are arrayed in a matrix on the substrate, each of the driving transistors having a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain;
> a plurality of signal lines which are patterned together with the gates of said plurality of driving transistors and arrayed to run in a predetermined direction on the substrate;
> a plurality of supply lines which are patterned together with the sources and drains of said plurality of driving transistors and arrayed to cross said plurality of signal lines via the gate insulating film, one of the source and the drain of each of the driving transistors being electrically connected to one of the supply lines; and
> a plurality of feed interconnections which are formed on said plurality of supply lines along said plurality of supply lines, respectively.

117. Claim 13 recites:

13. A display panel comprising:
a substrate;
a plurality of driving transistors which are arrayed in a matrix on the substrate, each of the driving transistors having a gate, a source, a drain, and a gate insulating film inserted between the gate, and the source and drain;
a plurality of signal lines which are patterned together with the gates of said plurality of driving transistors and arrayed to run in a predetermined direction on the substrate;
a plurality of supply lines which are patterned together with the sources and drains of said plurality of driving transistors and arrayed to cross said plurality of signal lines via the gate insulating film, one of the source and the drain of each of driving transistors being electrically connected to one of the supply lines;
a plurality of feed interconnections which are connected to said plurality of supply lines along said plurality of supply lines;
a plurality of pixel electrodes each of which is electrically connected to the other of the source and the drain of a corresponding one of said plurality of driving transistors;
a plurality of light-emitting layers which are formed on said plurality of pixel electrodes, respectively; and
a counter electrode which covers said plurality of light-emitting layers.

118. For the reasons discussed below, in my opinion, the meaning of "feed interconnections" is "conductive structures in a layer or layers different from the gates, sources and drains that provide connections to a source that supplies voltage and/or current."

119. The term "feed interconnections" is not a common or established term to a POSITA, and I cannot recall having seen the term used outside of the context of Casio's patents.

120. The specification discloses "feed interconnections [that] are stacked on supply lines" and "formed separately for [sic:from] the drains, sources, and gates of the driving transistor." '068 patent at 3:61-4:3; 4:10-14. The specification discloses that because the feed interconnections are formed separately from the transistors' drains, sources, and gates, the feed interconnections can be made thick and the resistance of the feed interconnect can be reduced compared to an interconnect or supply line formed in the TFT electrodes. *Id.*; *see also id.* at 1:57-2:35, 10:25-32,

18:26-40, 26:61-66. This provides a low resistance path for current to flow from the voltage source to the pixels and suppresses "voltage drop and signal delay." *Id.* at 3:61-4:3; 4:10-14, 10:25-32, 18:26-40, 26:62-66.

121. In every embodiment of the '068 patent, the feed interconnections are expressly formed in a layer different than the gates, sources and drains of the transistors. '068 patent at 10:25-32 ("feed interconnections 90 above formed by electroplating and are therefore much thicker than the signal lines Y_1 to Y_n, scan lines X_1 to X_m, supply lines Z_1 to Z_m, and the gates, sources, and drains of the transistors 21 to 23."); *see also id.* at 26:62-66 (same).

122. For example, annotated Figure 8 below shows that, in the first embodiment, the feed interconnections 90 (yellow) are formed above the gate layer (red) and source and drain layer (blue).in

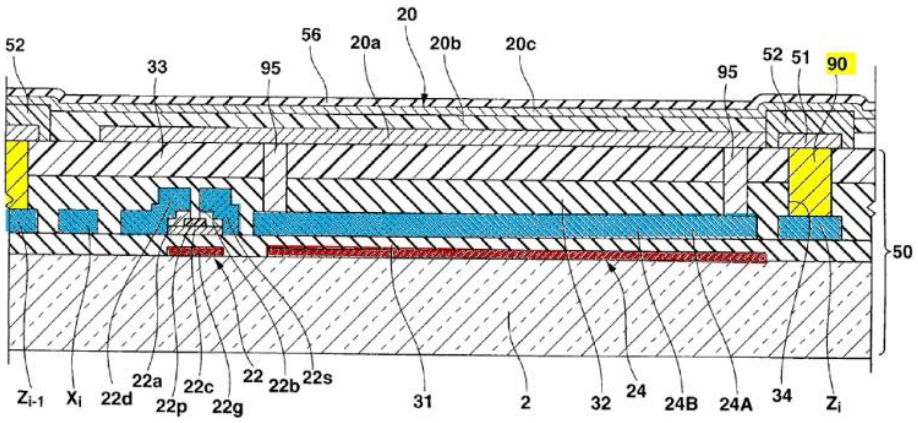


FIG.8

'068 patent at Fig. 8 (annotated).

123. Similarly, annotated Figure 25 below shows that, in the second embodiment, the feed interconnections 90 (yellow) are formed above the gate layer (red) and sources and drains layer (blue).

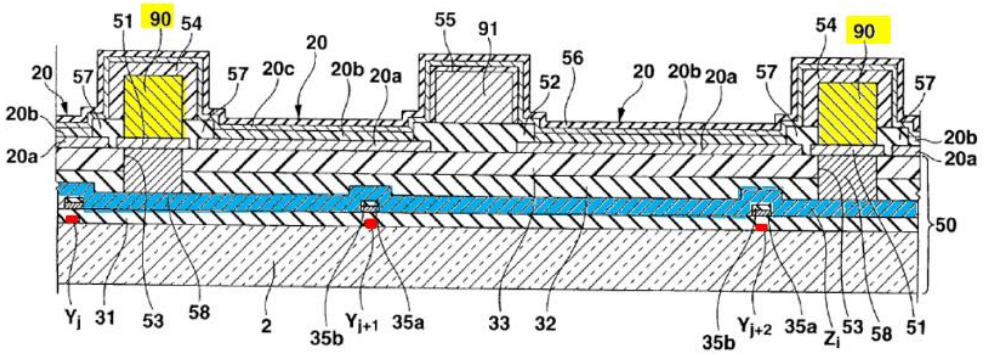


FIG.25

'068 patent at Fig. 25 (annotated).

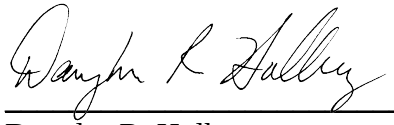
124. The specification teaches that it is because the feed interconnections are "formed from a conductive layer different from the gates, sources and drains of thin-film transistors" that the "voltage drop by the feed interconnections 90 is small" and "the write current (pull-out current) can sufficiently be supplied without any delay." '068 patent at 18:30-39; *see also id.* at 10:25-32, 26:61-66, Figs. 8, 25. A POSITA would have understood that this was important and a requirement of the claim because the "object of the present invention [is] to satisfactorily drive a light-emitting element while suppressing any voltage drop and signal delay." *Id.* at 2:38-41.

125. Furthermore, A POSITA would have been discouraged from forming the feed interconnections in the same layer as the TFT gates, sources or drains as discussed above with respect to limitation C.1 above .

126. It is my opinion that these statements in the prosecution history would have informed a POSITA that feed interconnections would need to be formed in a layer different than the gates, sources, and drains of the transistors.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 101 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.



Douglas R. Holberg

13 March 2020

Date

APPENDIX A

Douglas R. Holberg, Ph.D.
820 Camino de Rancho, Wimberley, TX. 78676 (512) 970-4007 ip@holberg.org

Education

B.S.E.E. - 1977, Texas A&M University, College Station, TX.

M.S.E. - 1989, The University of Texas, Austin, TX.

Ph.D. - 1992, The University of Texas, Austin, TX.

Experience

Intellectual Property Technical Consultant –

Apr 2013 – Present: Principal

- Patent analysis for licensing and litigation (offensive and defensive)
- Patent analysis and review for valuation
- Inter Partes Review
- Expert witness
- Teardown, electrical measurements and analysis
- Simulation and modeling
- Technical consulting

Jan 2008 – Mar 2013

- Patent analysis for licensing and litigation (offensive and defensive)
- Technical support for patent prosecution
- Patent analysis and review for valuation

Silicon Laboratories –

Jun 2005 – Jan 2008: V. P. of Technology

Dec 2003 – Jun 2005: Director of Engineering, MCU Products

Cygnal Integrated Products - Feb. 1999 to Dec 2003 (acquired by Silicon Labs Dec 2003)

Vice President of Engineering, Chief Technical Officer, Co-founder

Concurrent to the position at Cygnal, I served as Adjunct Assistant Professor at the University of Texas at Austin, and Technical Advisory Boards for Silicon Metrics and Celite Systems.

Adjunct Assistant Professor, University of Texas as Austin – 1995-2001

Taught “CMOS Analog Circuit Design” Graduate class: EE397K and Undergraduate class: EE338L

Crystal Semiconductor Corp. (Cirrus Logic) - Sep. 1996 to Feb. 1999

Director of Imaging and Video Products (CCD interface, CMOS imagers, TV encoders, etc.)

Crystal Semiconductor Corp. (Cirrus Logic) - Oct. 1992 to Sep. 1996

Design Manager for VLSI mixed-signal products including telecommunications and disk drive read channel devices.

Independent Consultant - Aug. 1987 to Oct. 1992

Taught a short-course entitled “CMOS Analog Integrated Circuit Design” in Berlin, Germany twice per year as a part of the “Berlin Continuing Engineering Education Program.” In addition, this course was taught at Analog Devices BV, Ireland, Aug. 1990.

Lectured at Baylor University's Department of Engineering (Spring ‘89, Spring ‘91).

Consultant for Advanced Micro Devices, Crystal Semiconductor, and other companies on projects relating to switched-capacitor filters, operational amplifiers, latchup, and the ISDN analog interface.

Crystal Semiconductor Corp. - Oct. 1984 to Aug. 1987

Project leader on the CS7008 Universal Filter--a universal programmable filter using novel switched-capacitor techniques. This design was completed in a 3µm silicon-gate double-polysilicon CMOS process.

Texas Micro Engineering, Inc. - June 1980 to Oct. 1984

Project leader on TME3030 Sense Amplifier/Filter--a dual-channel switched-capacitor filter circuit to be used in a medical electronic application. Co-designed a gate-array platform customized for medical and consumer products. Performed extensive device characterization of MOS transistors. This work included characterization of noise performance and characterization of transistors operating in weak inversion.

Mostek, Inc., Carrollton, TX. - Jan. 1978 to June 1980

Circuit designer. Served as project leader on MK5387 DTMF generator.

Inventions

1.	10,492,686	Devices, systems and methods for using and monitoring medical devices
2.	8,010,819	Microcontroller unit (MCU) with power saving mode
3.	7,719,595	Preview mode low resolution output system and method
4.	7,660,968	Reconfigurable interface for coupling functional input/output blocks to limited number of I/O pins
5.	7,613,901	Comparators in IC with programmably controlled positive / negative hysteresis level and open-drain/push-pull output coupled to crossbar switch or rising/falling edge interrupt generation
6.	7,511,465	Digital pulse width modulated power supply with variable LSB
7.	7,504,902	Precision oscillator having linbus capabilities
8.	7,504,900	Integrated circuit package including programmable oscillators
9.	7,502,883	USB integrated module
10.	7,498,962	Analog-to-digital converter with low power track-and-hold mode
11.	7,441,131	MCU with power saving mode
12.	7,421,251	Precise frequency generation for low duty cycle transceivers using a single crystal oscillator
13.	7,382,181	Method and apparatus for tuning GMC filter
14.	7,323,855	Digital pulse width modulated power supply with variable LSB
15.	7,315,200	Gain control for delta sigma analog-to-digital converter
16.	7,304,679	Preview mode low resolution output system and method
17.	7,289,145	Correlated double sampling variable gain amplifier circuit for use in a digital camera
18.	7,286,176	CCD imager analog processor systems and methods
19.	7,256,611	Cross-bar matrix with LCD functionality
20.	7,171,542	Reconfigurable interface for coupling functional input/output blocks to limited number of i/o pins
21.	7,164,311	Method and apparatus for tuning GMC filter
22.	7,061,421	Flash ADC with variable LSB
23.	6,950,047	Method and apparatus for combining outputs of multiple DACs for increased bit resolution
24.	6,922,164	SAR analog-to-digital converter with abort function
25.	6,891,487	Capacitor calibration in SAR converter
26.	6,879,004	High voltage difference amplifier with spark gap ESD protection
27.	6,724,336	Segmented D/A converter with enhanced dynamic range
28.	6,720,999	CCD imager analog processor systems and methods
29.	6,686,957	Preview mode low resolution output system and method
30.	6,617,934	Phase locked loop circuits, systems, and methods
31.	6,448,917	DAC using current source driving main resistor string
32.	6,400,300	D/A converter street effect compensation
33.	6,384,763	Segemented D/A converter with enhanced dynamic range
34.	6,288,661	A/D converter with voltage/charge scaling
35.	6,285,536	High voltage input pad system
36.	6,172,361	Methods for mounting an imager to a support structure and circuitry and systems embodying the same
37.	6,038,116	High voltage input pad system
38.	4,849,662	Switched-capacitor filter having digitally-programmable capacitive element
39.	4,492,927	Offset voltage compensation circuit
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Other Professional Activities

Served on the "Industrial Electronics Advisory Committee" for the University of Texas Instruction and Materials Center, University of Texas, Austin, 1988-1989.

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